Paolo Mirone

Tutor: Prof. Andrea Irace

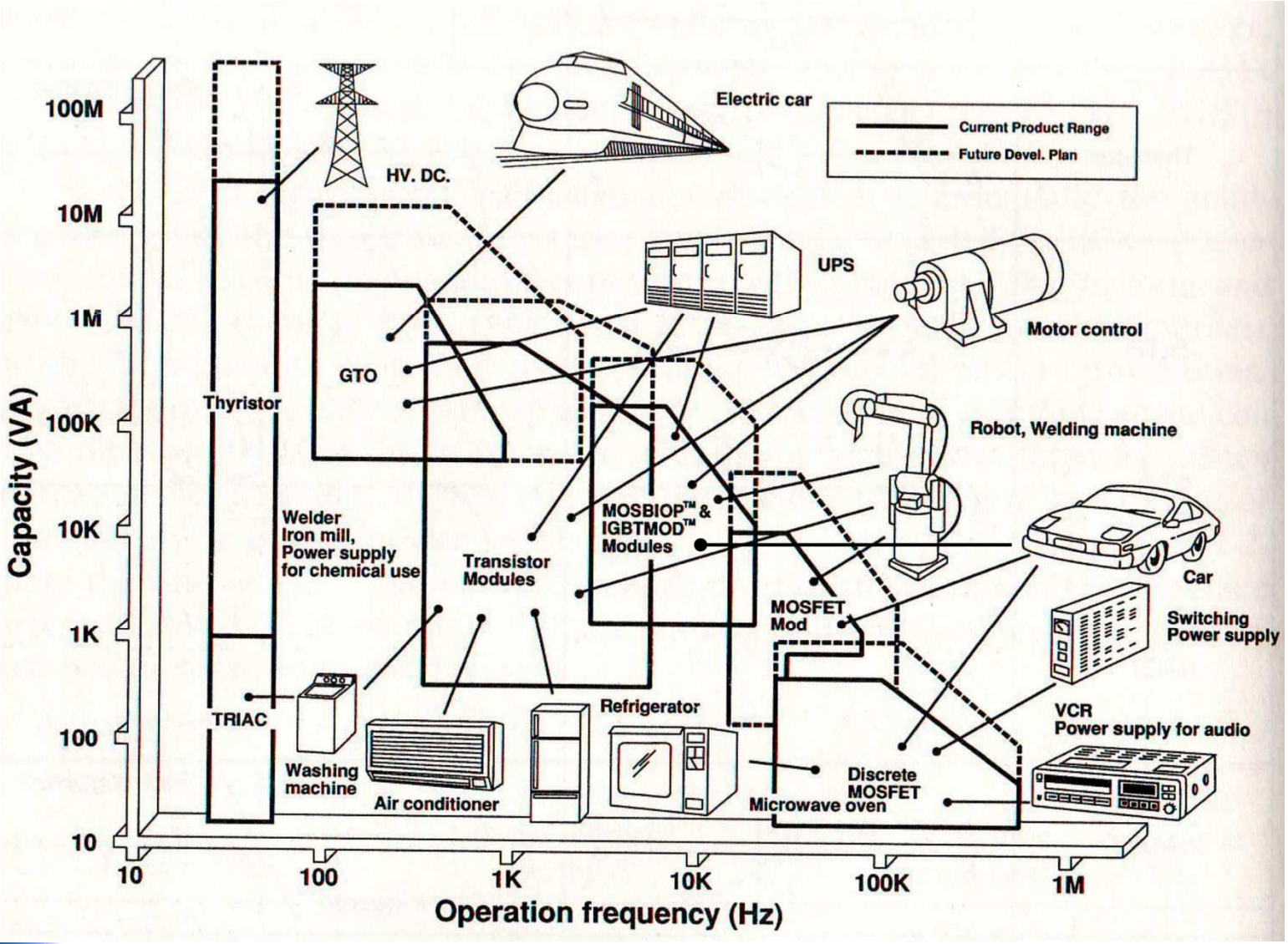
XXIX Cycle - III year presentation

Advanced termination structures for HV Power Semiconductor Devices

Background

- Paolo Mirone received B.S. (2010) and M.S. (2013) degrees in Electronic Engineering from the University of Naples "Federico II".
- He is currently PhD Student with the Department of Electrical Engineering and Information technologies (DIETI) at University of Naples "Federico II".
- His tutor is the Prof. Andrea Irace.
- His research interests include modeling, simulation and experimental characterization of Power Semiconductor Devices.
- His doctoral activities have been performed in collaboration with Vishay Semiconductor Italiana.

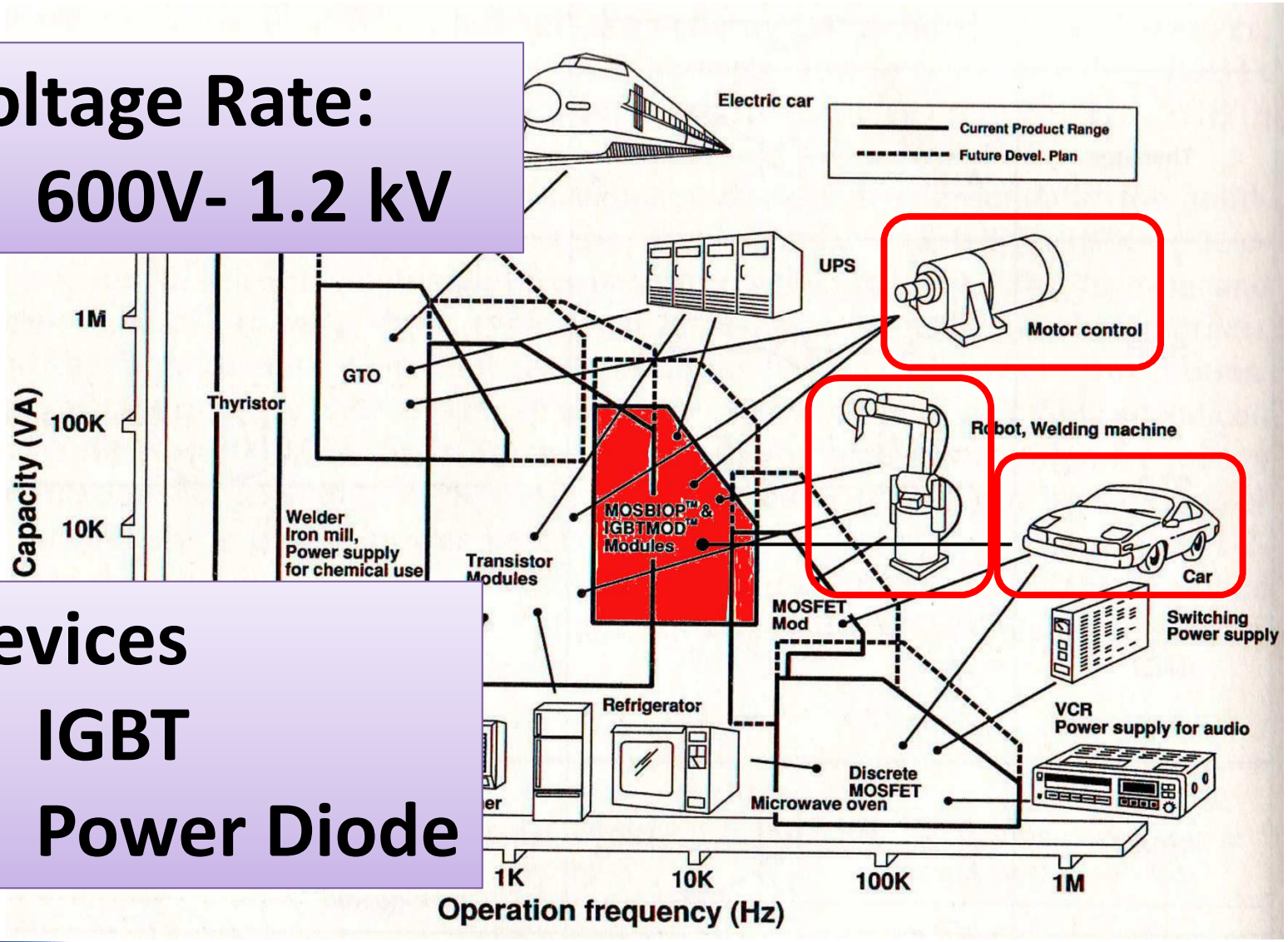
Context


Electric car
Current Product Range
Future Devel. Plan
HV. DC.
UPS
Motor control
GTO
Thyristor
Robot, Welding machine
MOSBIOP™ &
IGBTMOD™
Modules
Welder
Iron mill,
Power supply
for chemical use
Transistor
Modules
Car
MOSFET
Mod
Switching
Power supply
TRIAC
Refrigerator
VCR
Power supply for audio
Washing
machine
Air conditioner
Discrete
MOSFET
Microwave oven
Capacity (VA)
100M
10M
1M
100K
10K
1K
100
10
10
100
1K
10K
100K
1M
Operation frequency (Hz)

Context

Voltage Rate:

- **600V- 1.2 kV**



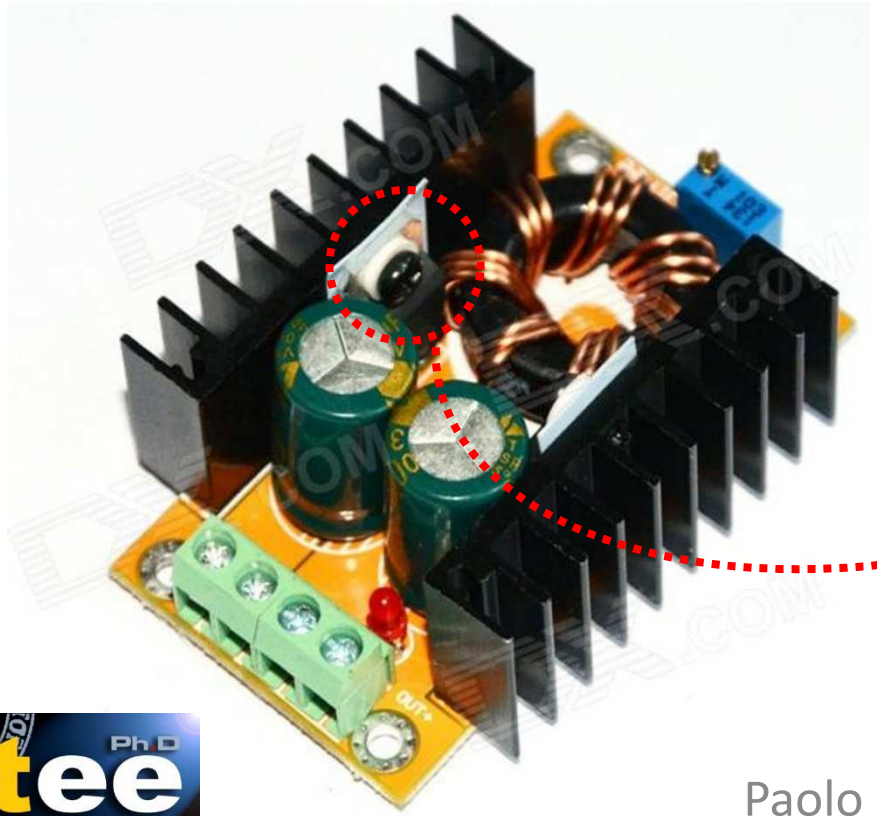
Devices

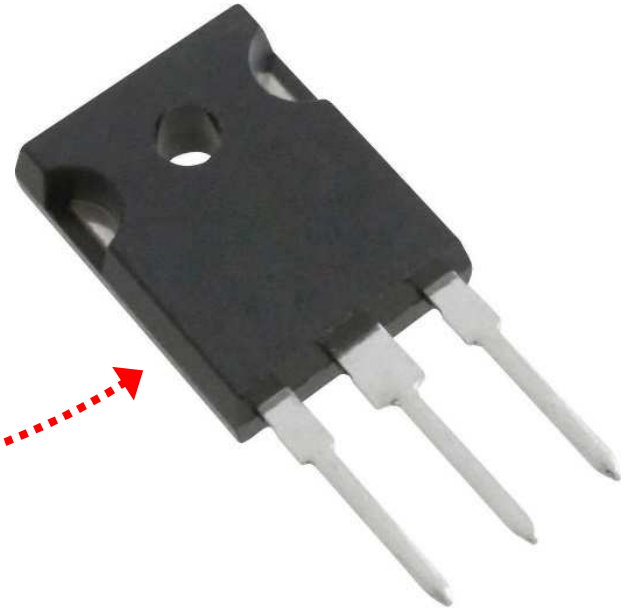
- **IGBT**
- **Power Diode**

Power Electronic

Power electronic is the key technology to reduce the consumption of energy by means of the enhancement of power conversion efficiency

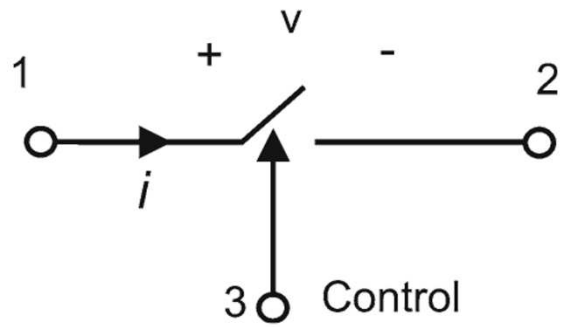
Boost Converter configuration

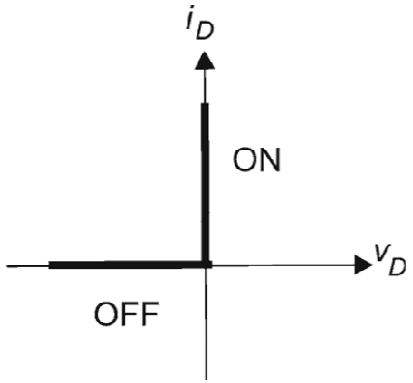




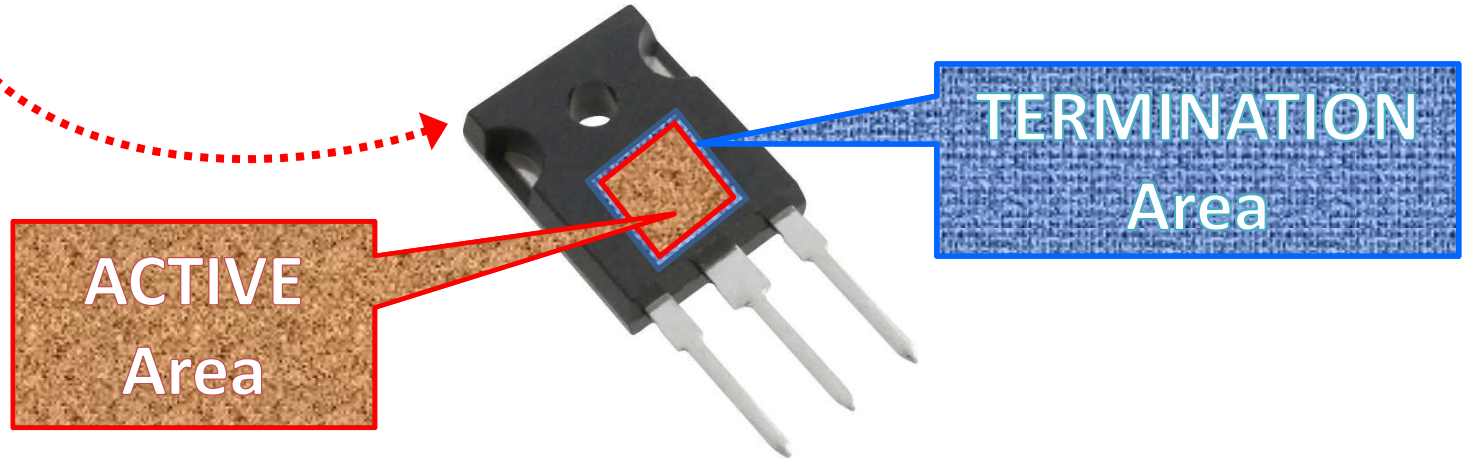
Power Devices

Power conversion system are constituted by Power Semiconductor Devices acting as Power Switch.





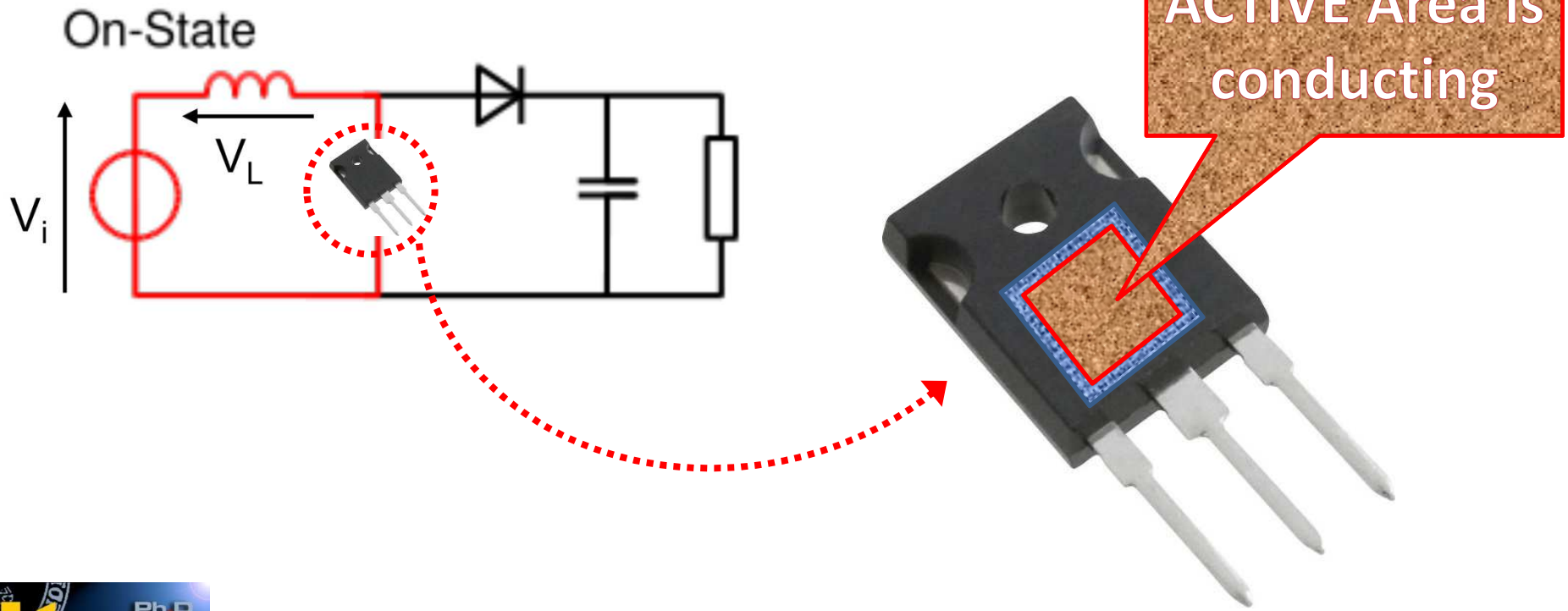
A **Switch** is composed by the **input**, the **output**, and a **control terminal** that imposes **ON/OFF** conditions on the switch



Conversion system (I)

Power electronic circuit are used to control the power conversion

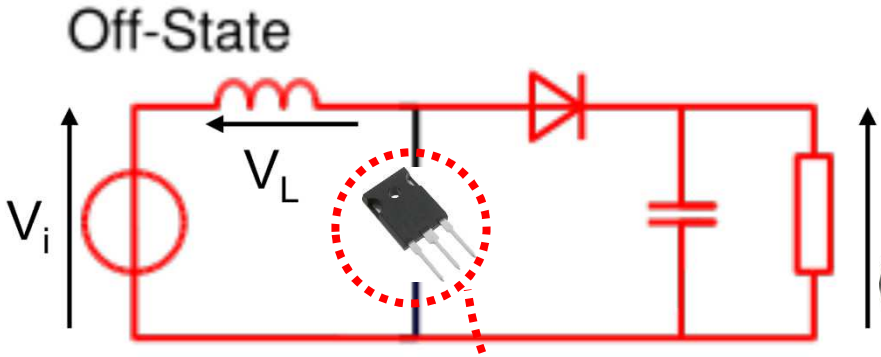
Boost Converter configuration

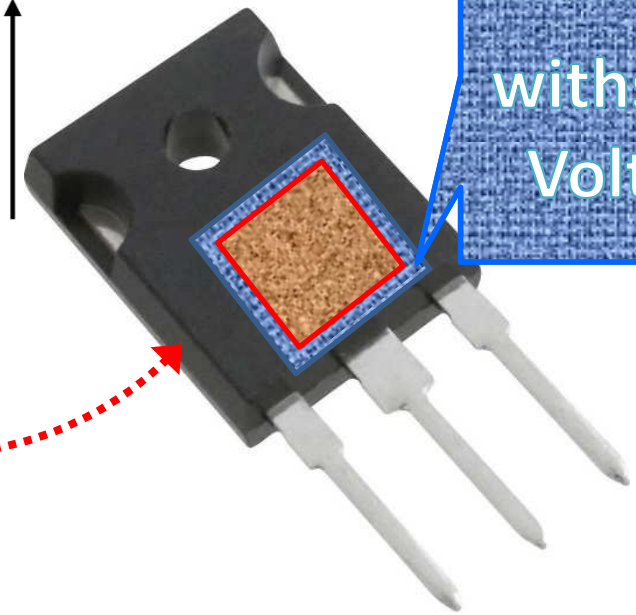


Conversion system (II)

Power electronic circuit are used to control the power conversion

Boost Converter configuration





TERMINATION Area withstands the Voltage Rate

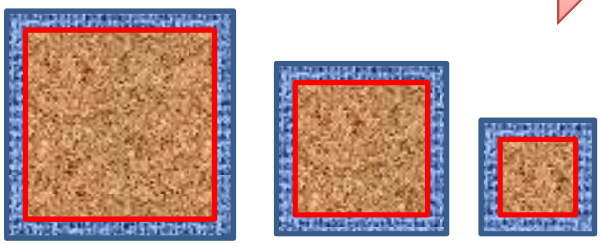
Motivations

Modern trend for Power devices tends to a technology scaling

Termination Area

Reduction of die size at constant the voltage rate leads to **reduction of the ratio** between *Active Area* and *Termination Area*

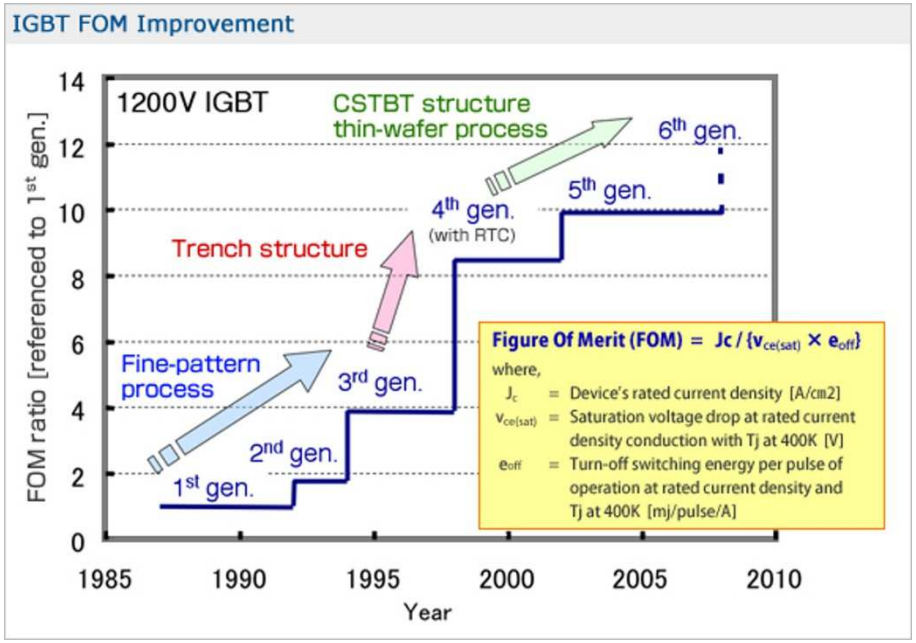
DIE SIZE



Solution**: New designs**

Problem**: reliability** and **ruggedness** requirements.

Active Area



Solution: Current density increment.

Problem: Thermal **Reliability**

Activities

Design of **new Termination structures** for 1.2kV Power Devices:

- **Parameters optimization Procedure.**
- **Ruggedness** analysis.
- Investigation on **current crowding** phenomena.
- **Process fabrication** emulation.

Short-Circuit capability analysis on Field Stop (FS)-IGBT devices:

- Experimental measurements
- New design proposal

Other activities:

- Study and analysis of state-of-art modern Power Devices:

  Reverse Conducting (RC)-IGBT

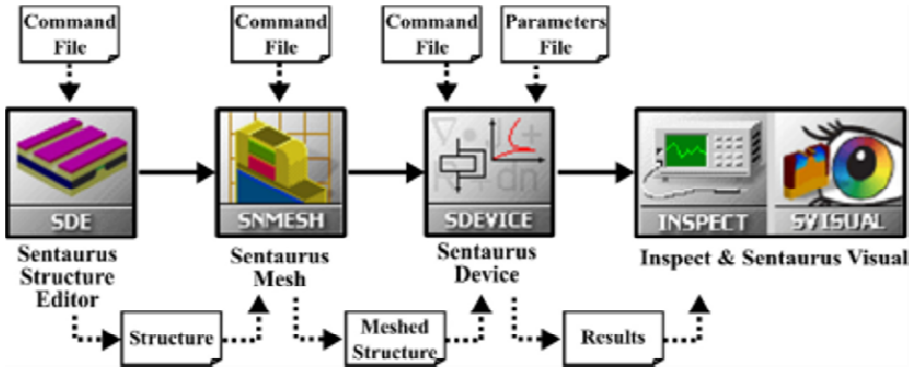
Approach

Termination Designs

Short-Circuit Analysis on Active Area

Sentaurus TCAD:

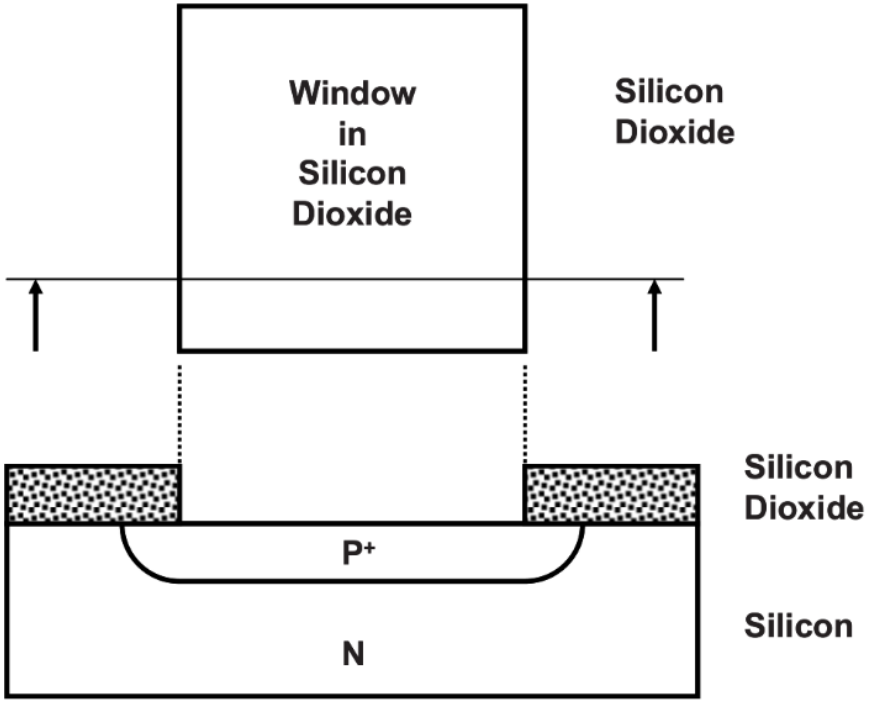
- Isothermal
- Electro-thermal simulations



Experimental characterization:

- Electrical measures
- UIS test
- ILS test
- Short-Circuit test

Edge Termination

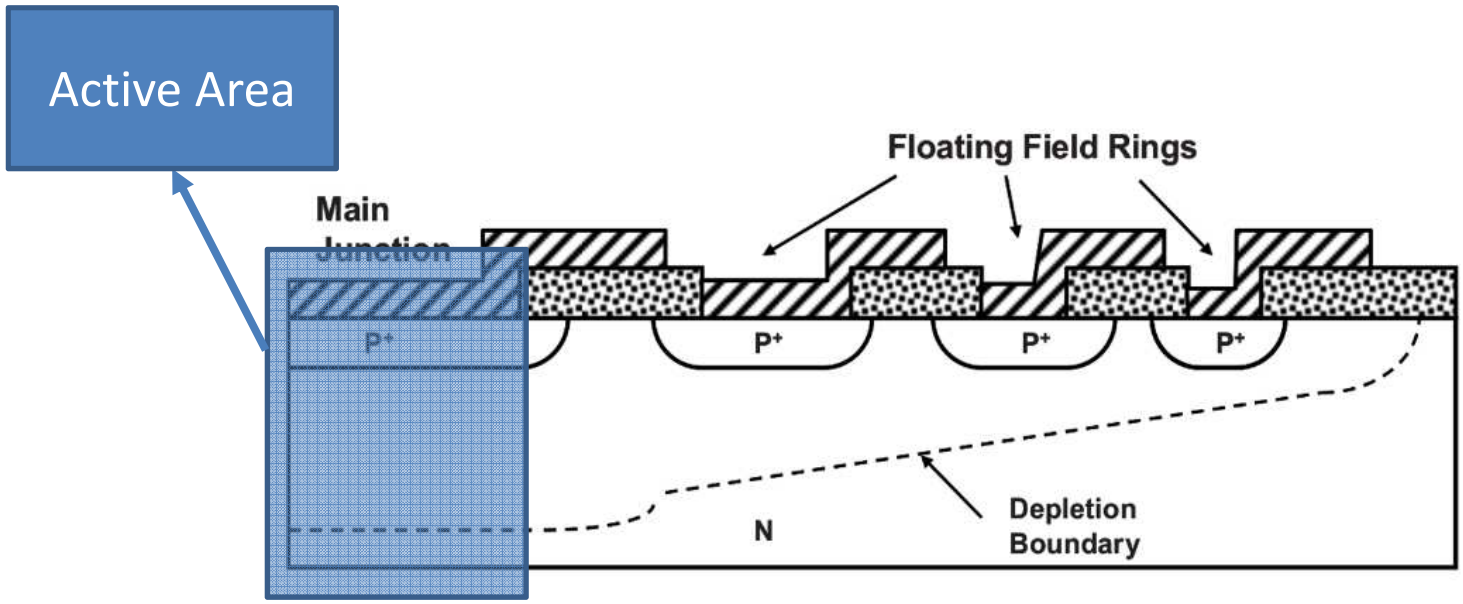


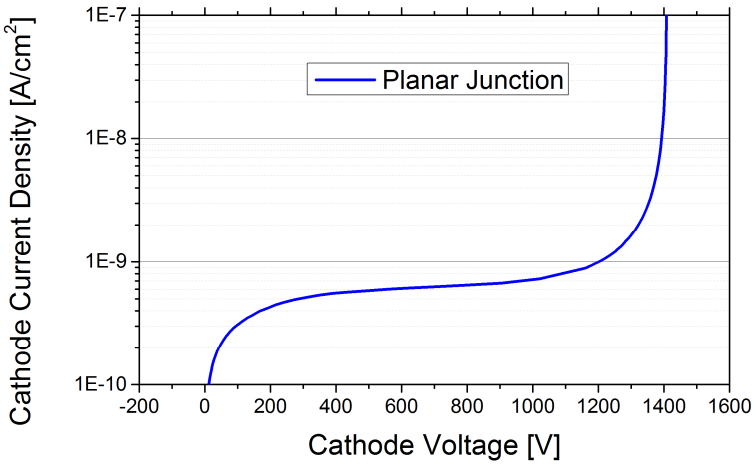
The **Avalanche Breakdown** phenomenon limits the **Voltage Rate** of the device

Termination must prevent the depletion region to meet the lattice damage:

- Increases the Leakage current.
- Reduces the Breakdown Voltage capability

Why the Termination ?





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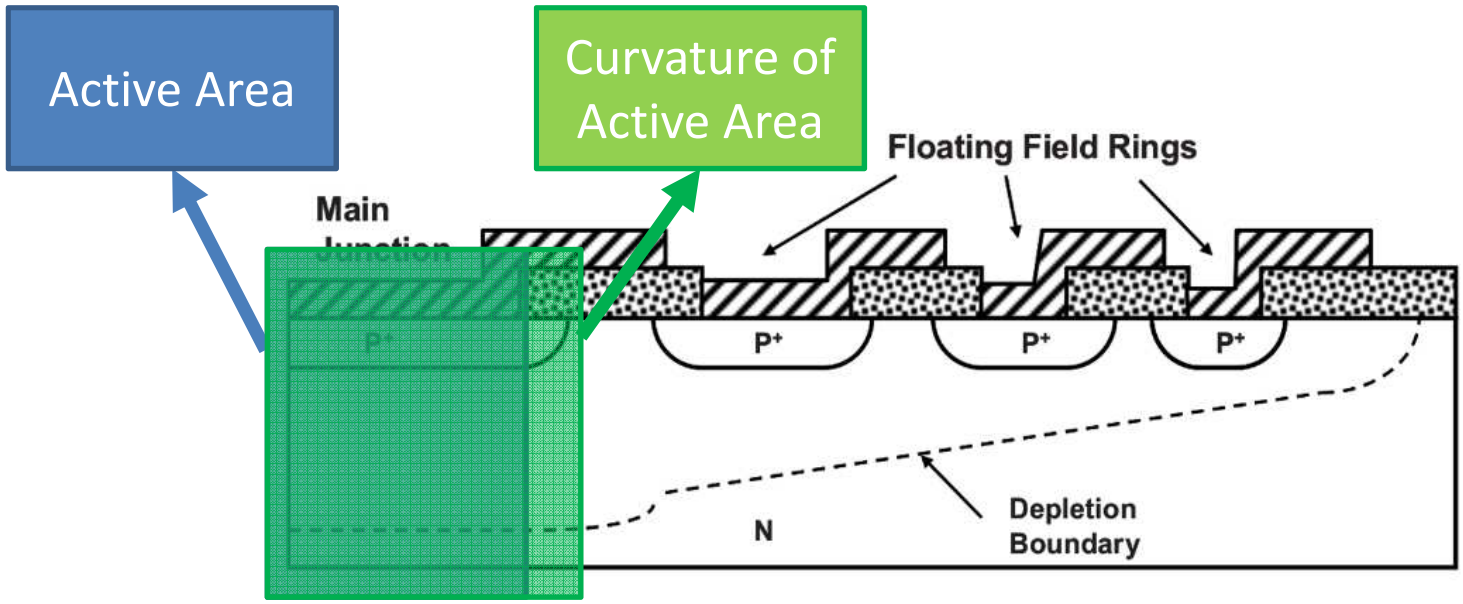
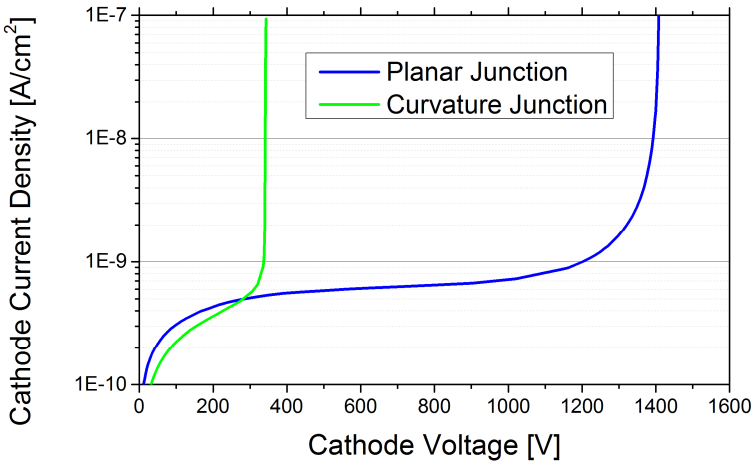
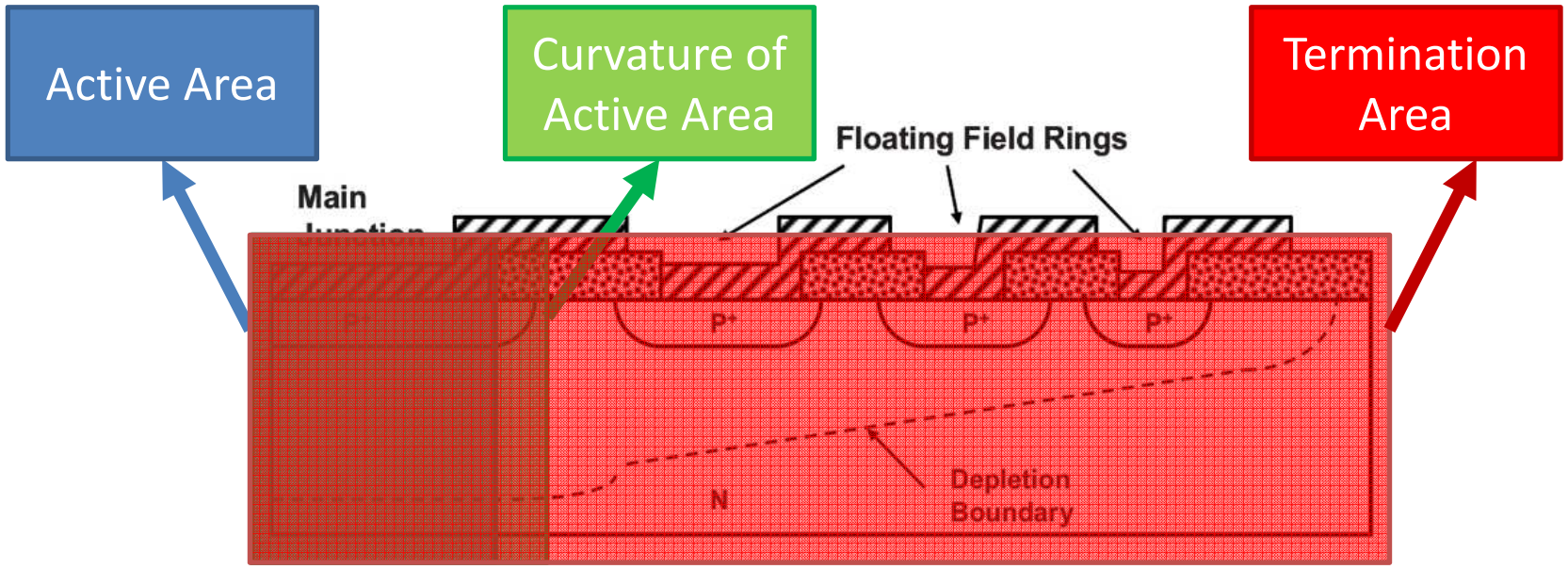
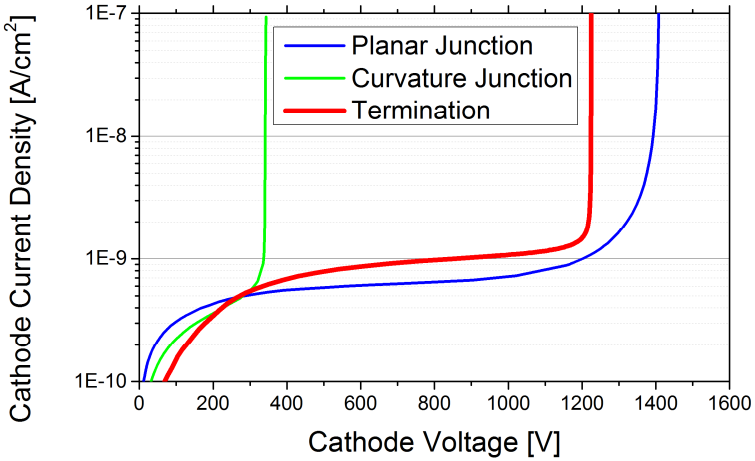


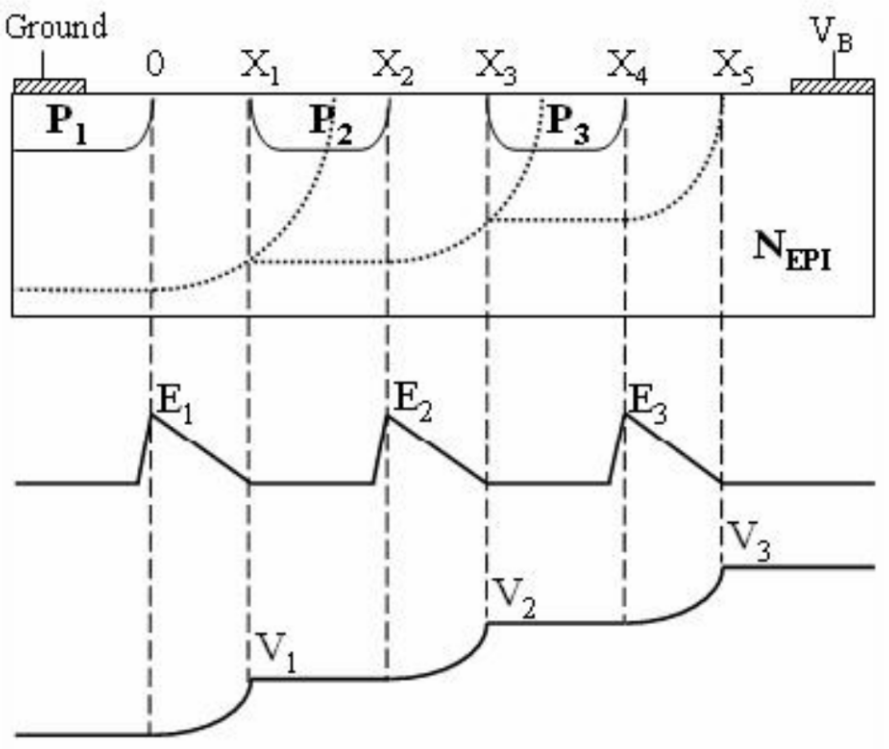


Why the Termination ?

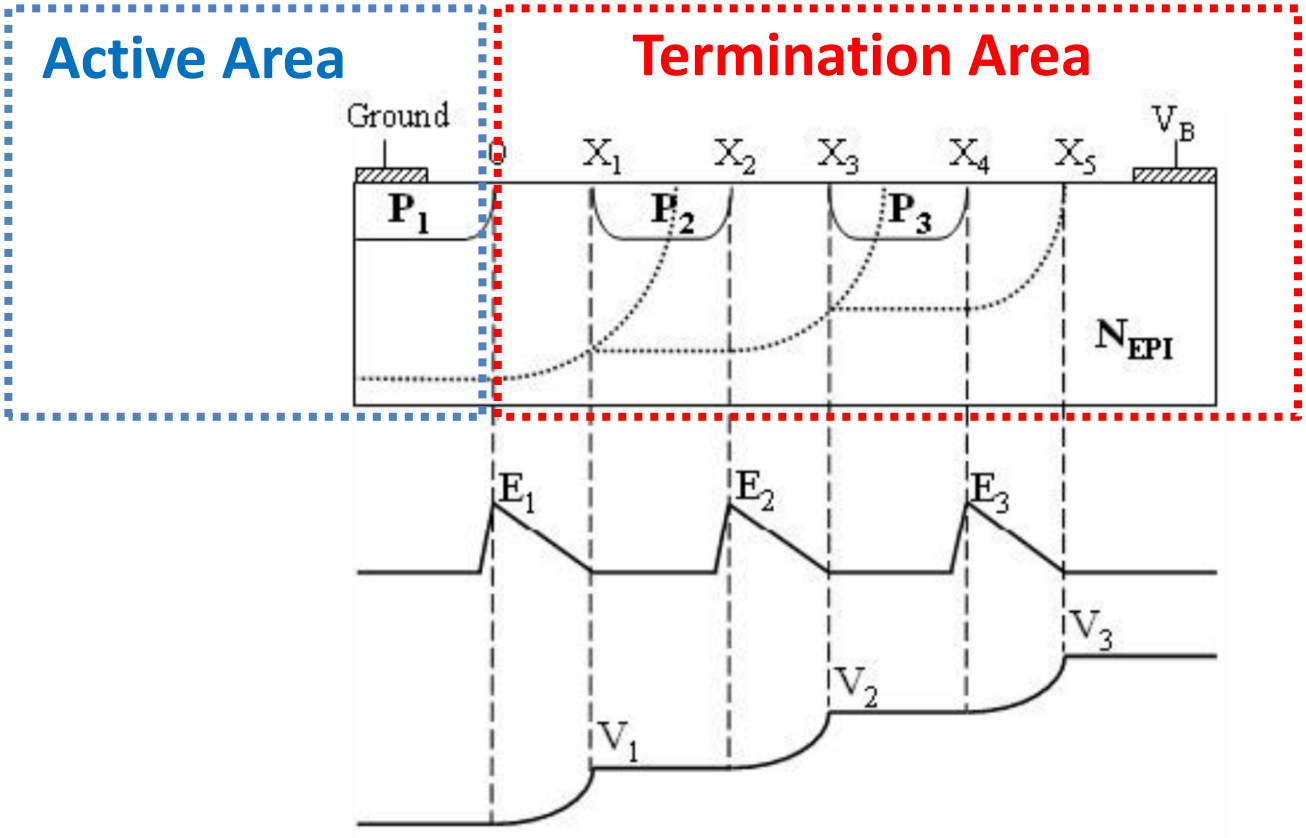




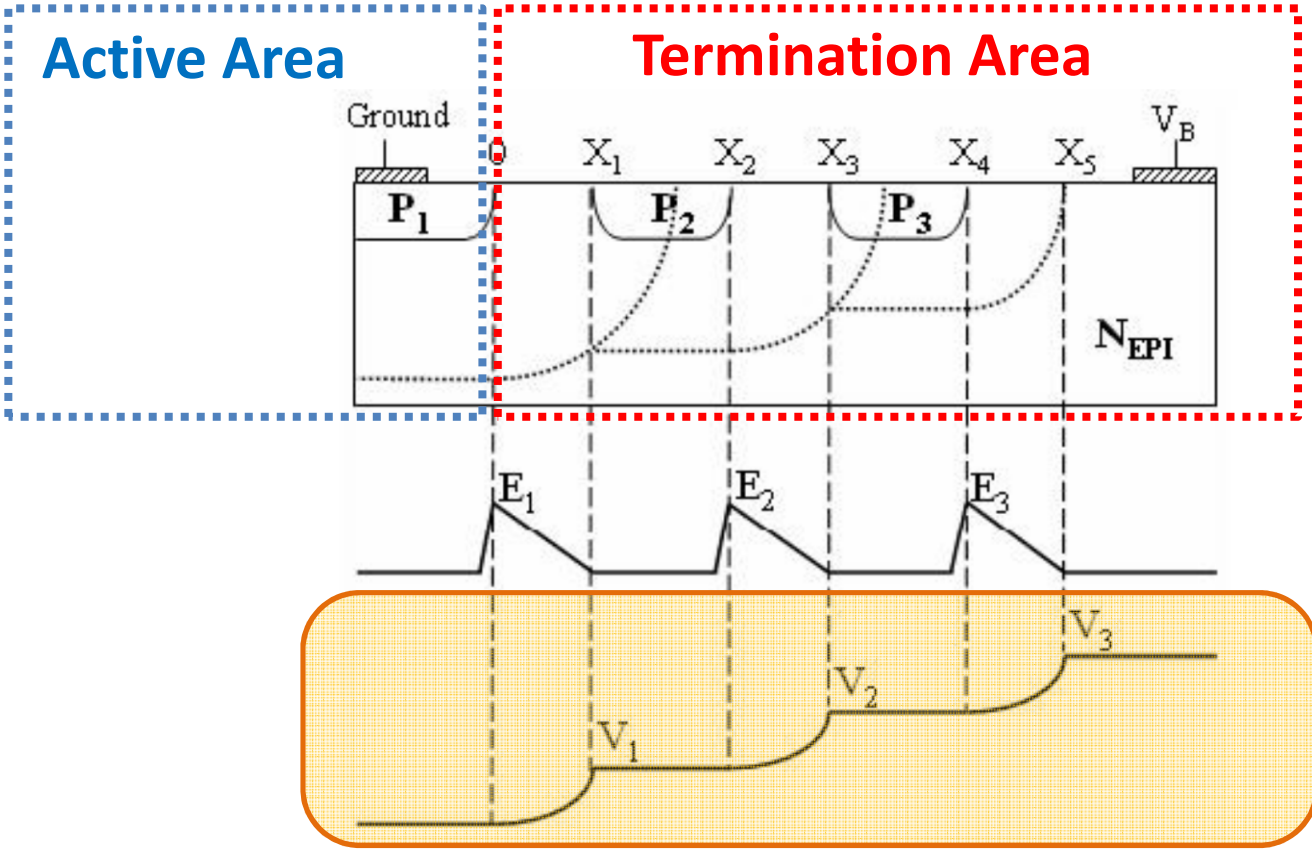
Termination Design Benefits



Termination Design Benefits

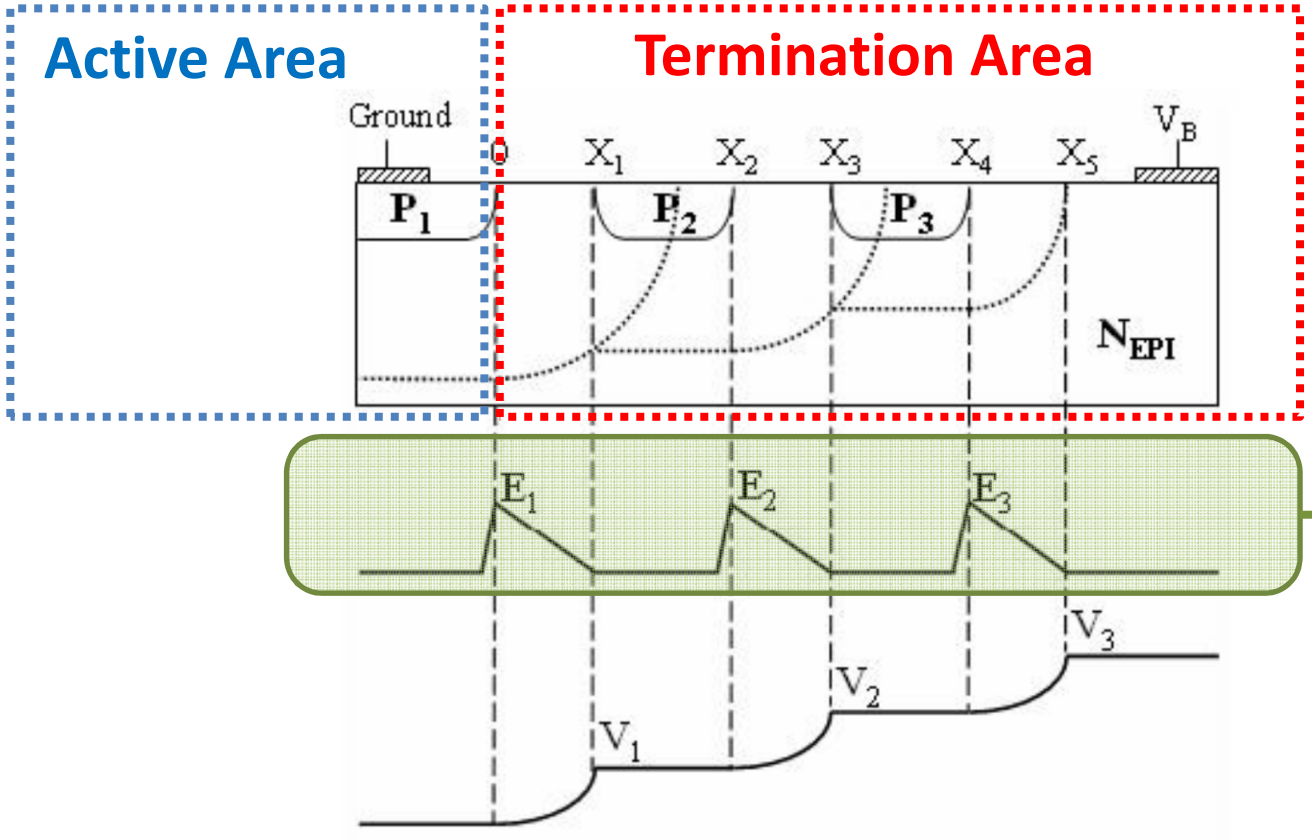


Termination Design Benefits



Electrostatic Potential distribution

Termination Design Benefits

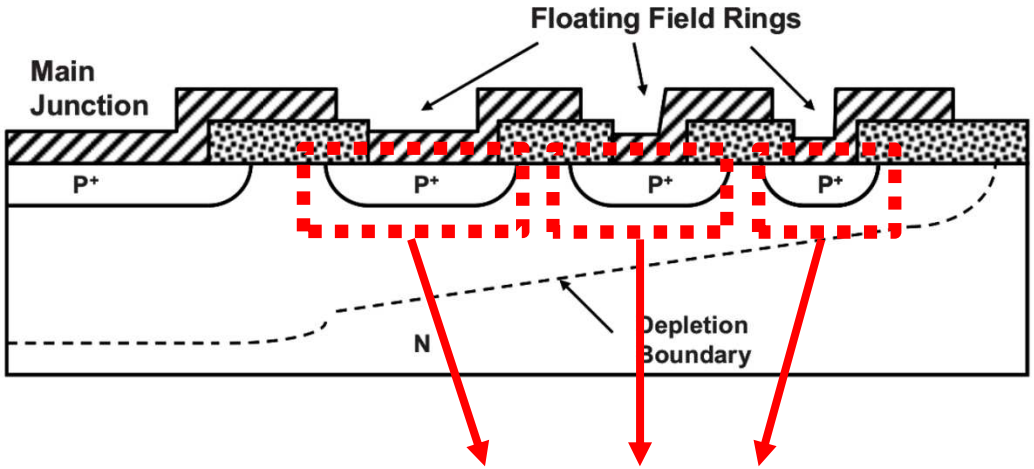


Electric Field distribution

Termination Techniques: FFR

During the years many techniques have been developed such as **Floating Field Ring (FFR), Field Plate, JTE, RESURF, SIPOS**

Floating Field Ring assisted by **Field Plate**



Floating Rings

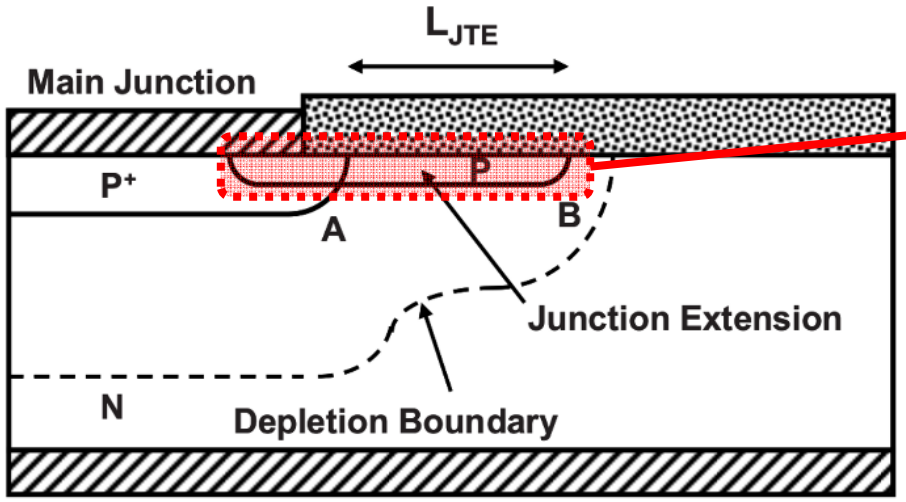
The potential along the termination depends on floating rings and field plates geometries

Termination Techniques: JTE

During the years many techniques have been developed such as **Floating Field Ring (FFR), Field Plate, JTE, RESURF, SIPOS**

Junction Termination Extension (JTE)

Advantage: Reduced occupation of area



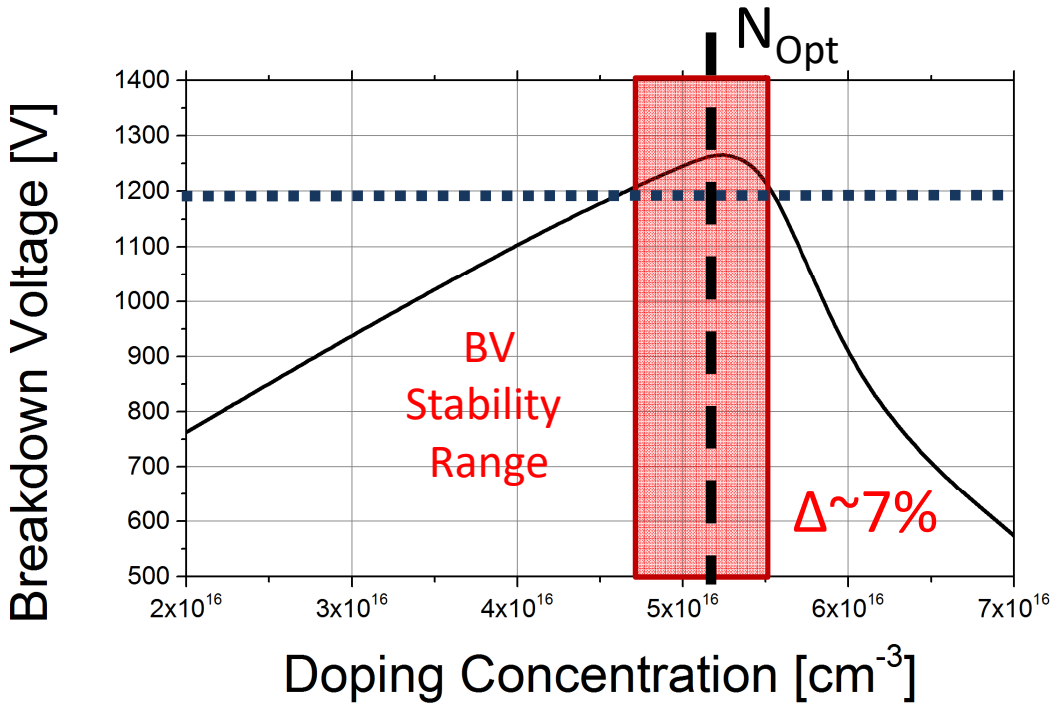
JTE Diffusion

The potential along the termination depends on **JTE Diffusion Length** (L_{JTE}), **JTE Diffusion doping profile**

JTE Termination Problem

Technological process fluctuation and/or the presence of impurities at the Silicon/Oxide interface can lead to Breakdown instability

Criticality: Sensitivity of the Breakdown Voltage (BV) to the *JTE Diffusion* doping profile



Target: To **enlarge** the *Breakdown Stability Range* of the termination to enhance the **Reliability requirements**.

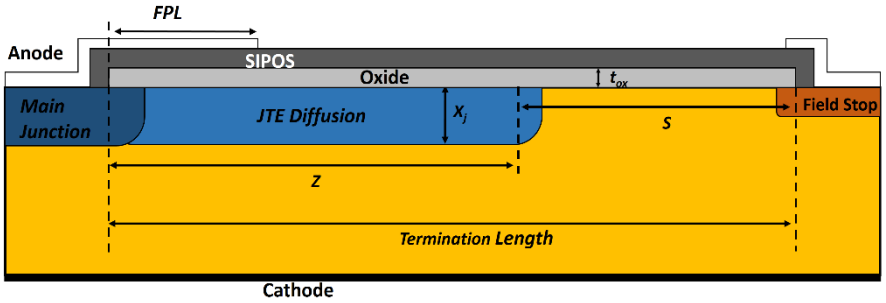
Specific Activity

New Termination Design:

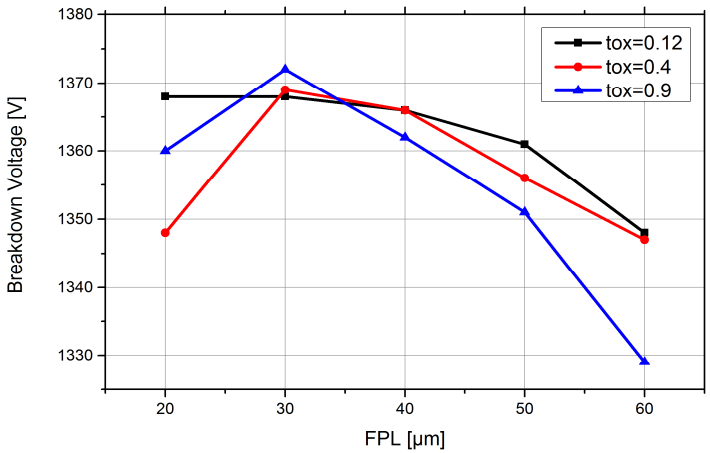
- SIPOS-JTE structure
- OGA-JTE structure

Design optimization procedure
to maximize the Breakdown Voltage capability

SIPOS-JTE Termination: Optimization (I)



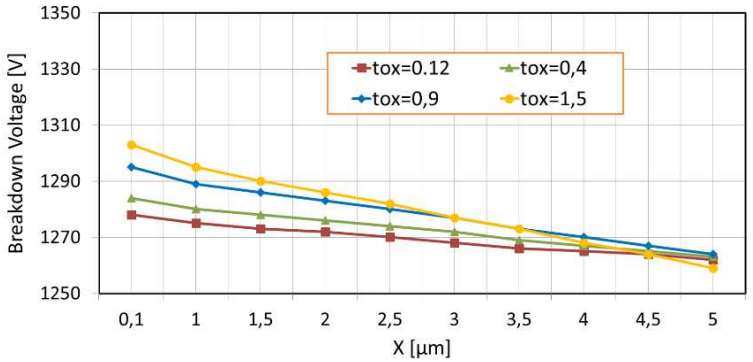
Field Plate Engineering



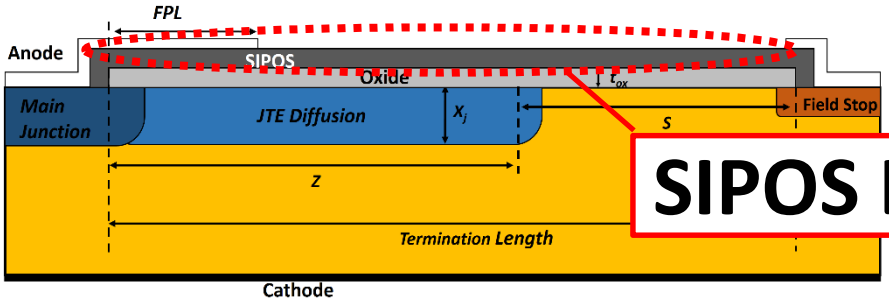
SIPOS-JTE parameters list and design rules.

Parameter	*Symbol*	*Range*
JTE Diffusion Length	*Z*	40-220 [µm]
Distance between JTE diffusions and field stop	*X*	0-5[µm]
Distance between JTE diffusions and field stop	*S*	100-280 [µm]
Oxide thickness	t_{ox}	1200-22000 [Å]
Field plate length	*FPL*	- [µm]
SIPOS Resistivity	ρ	$1x10^3$-$1x10^7$ [Ω·cm]
Termination length	*L*	250-300 [µm]

Breakdown Voltage Vs X distance

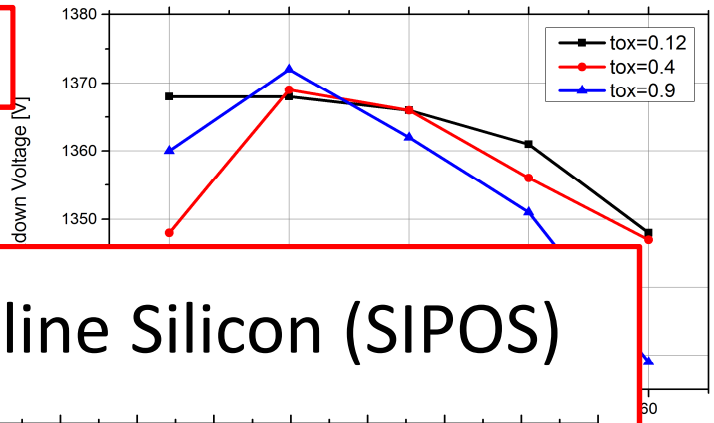


SIPOS-JTE Termination: Optimization (I)



SIPOS Layer

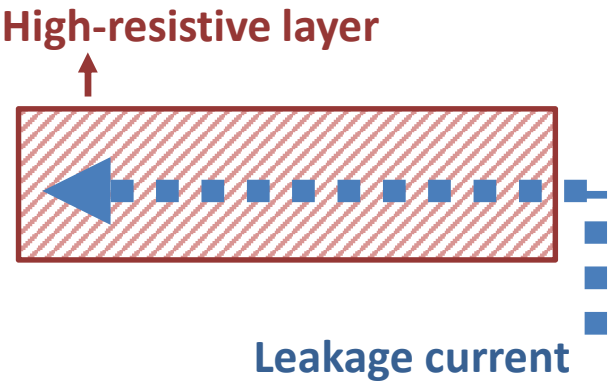
Field Plate Engineering

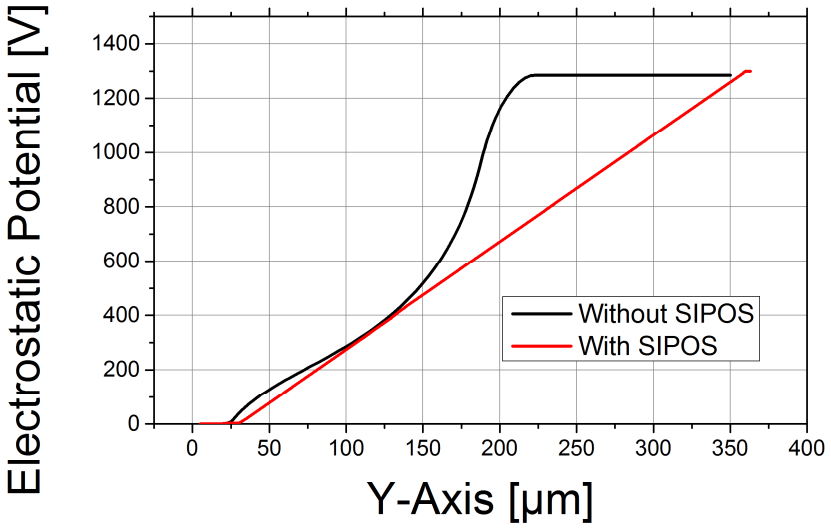


SIPOS-J

JTE I
Distance b
a
Distance b
a
Ox
Fie
SIP
Tern

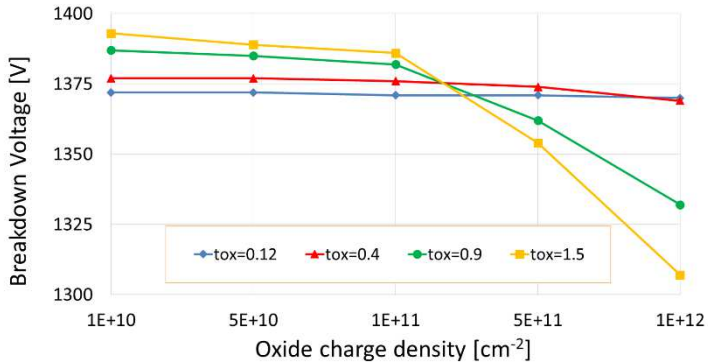
Semi-Insulating Polycrystalline Silicon (SIPOS)





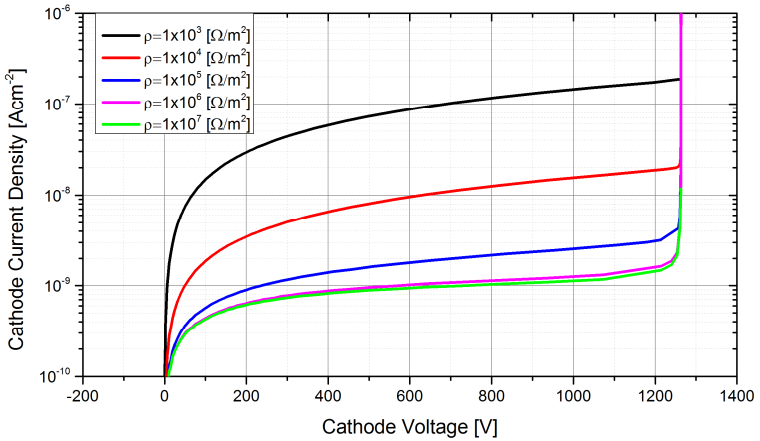
SIPOS-JTE Termination: Optimization (II)

BV Vs Oxide Charge density

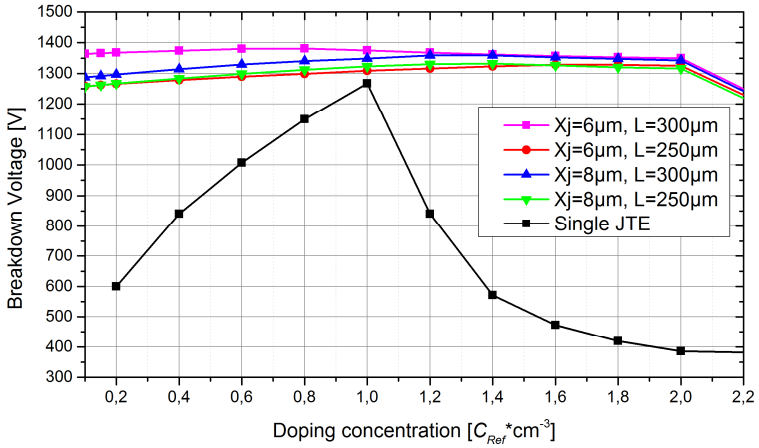


Great rejection against interface impurity, especially for thin oxide thickness

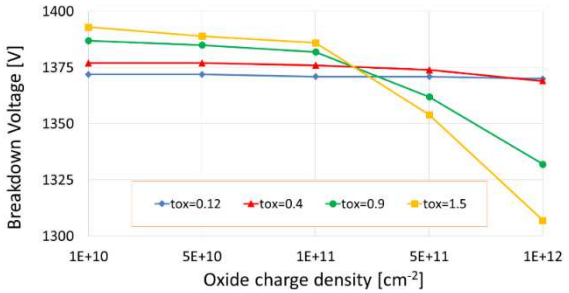
Leakage current Vs SIPOS resistivity



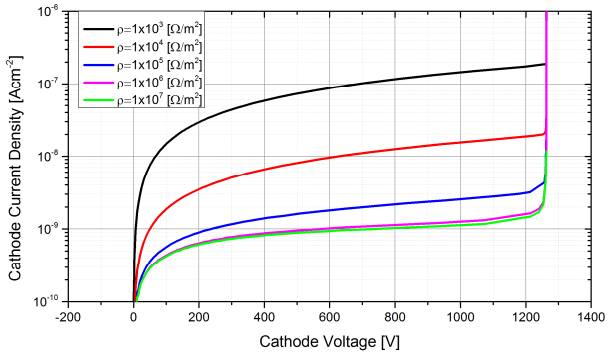
BV Vs JTE Doping Concentration

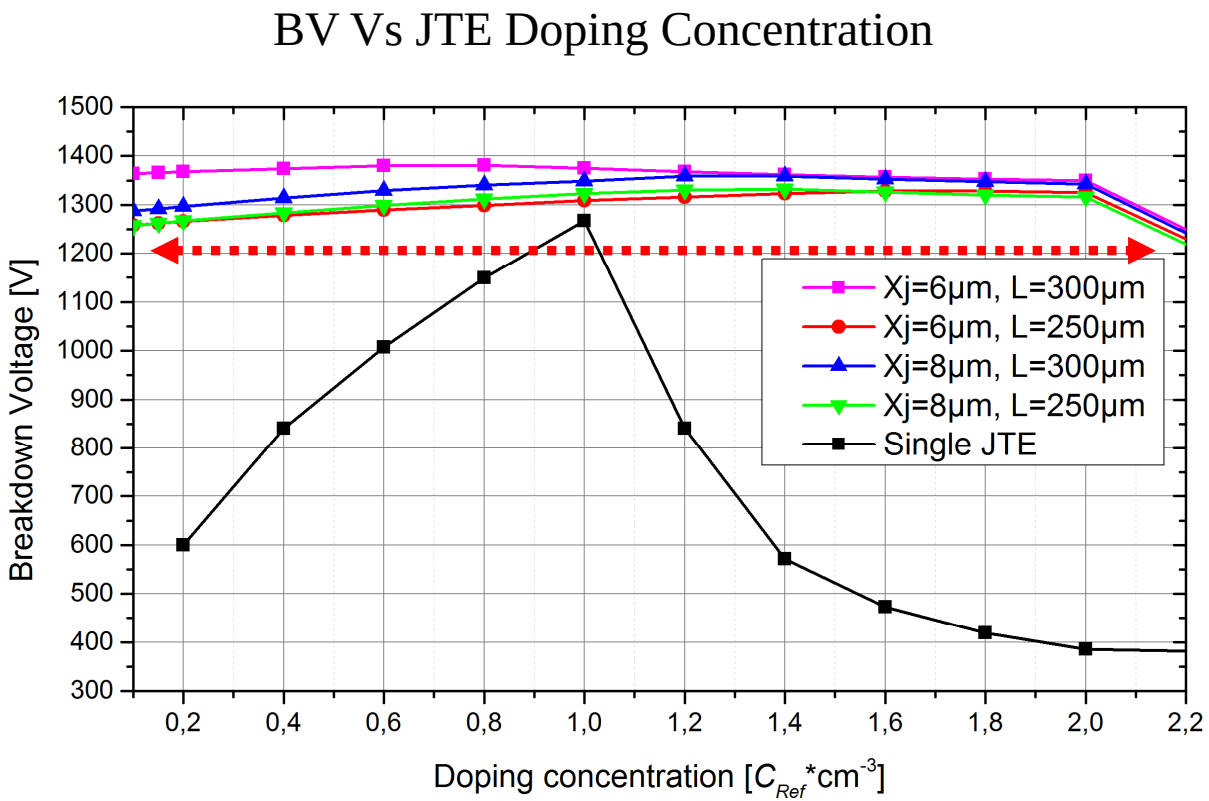


SIPOS-JTE Termination: Optimization (II)

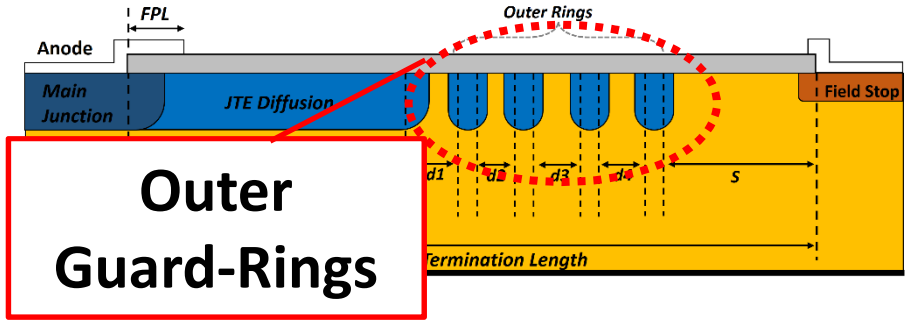


Breakdown Stability Range is considerably enlarged

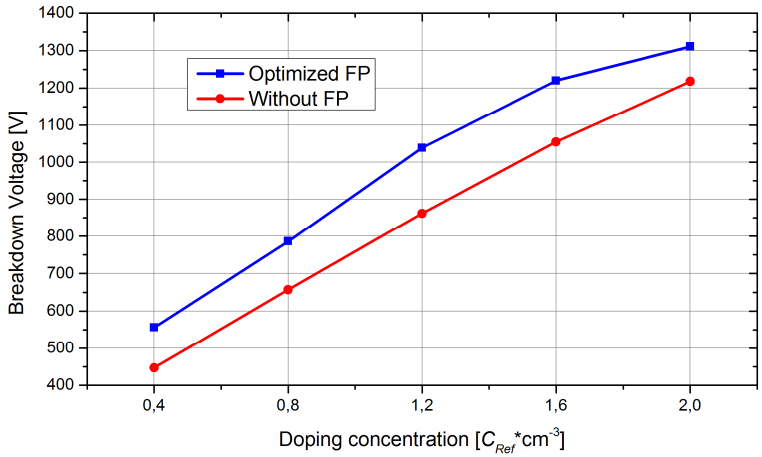




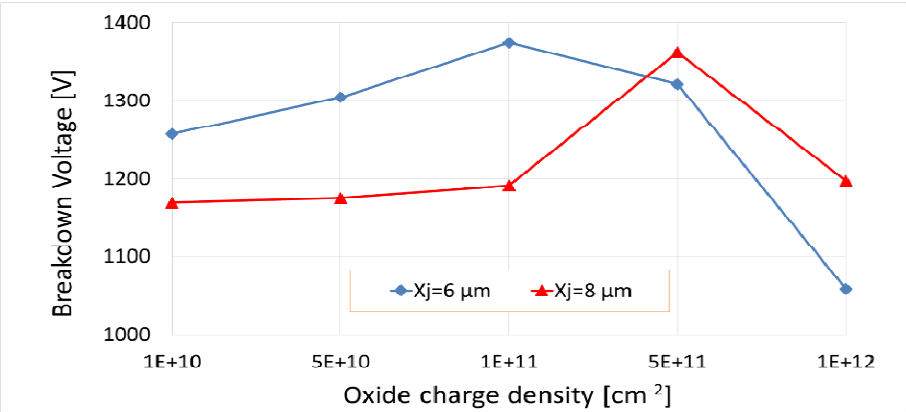
OGA-JTE Termination: Optimization (I)

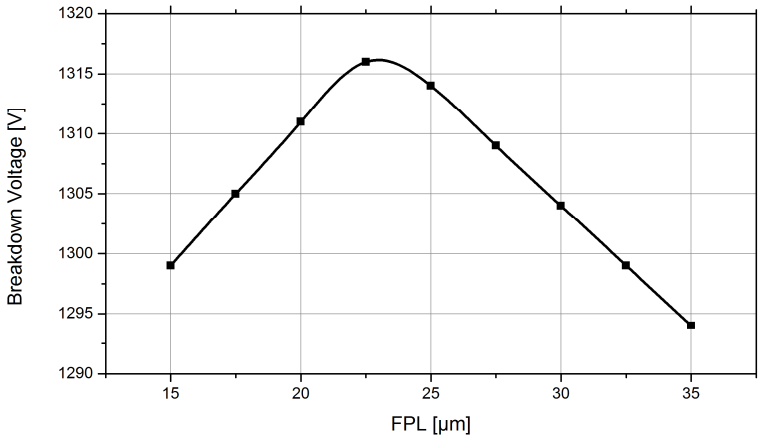


Field Plate Engineering



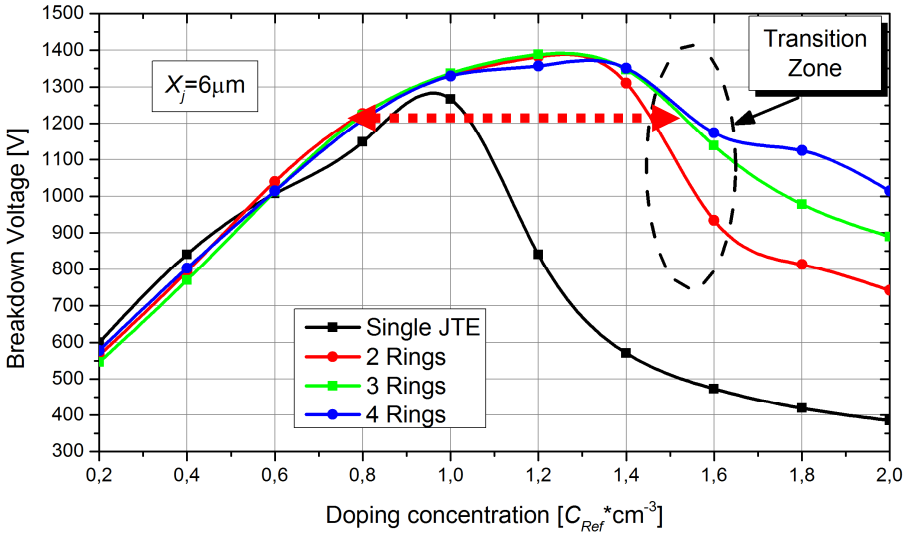
BV Vs Oxide Charge density



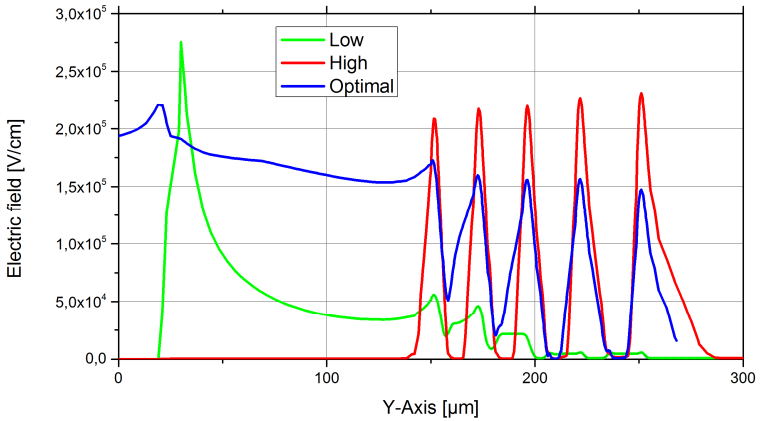


OGA-JTE Termination: Optimization (II)

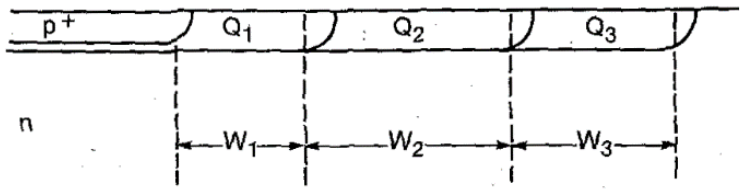
BV Vs JTE Doping Concentration



Superficial Electric Field distribution

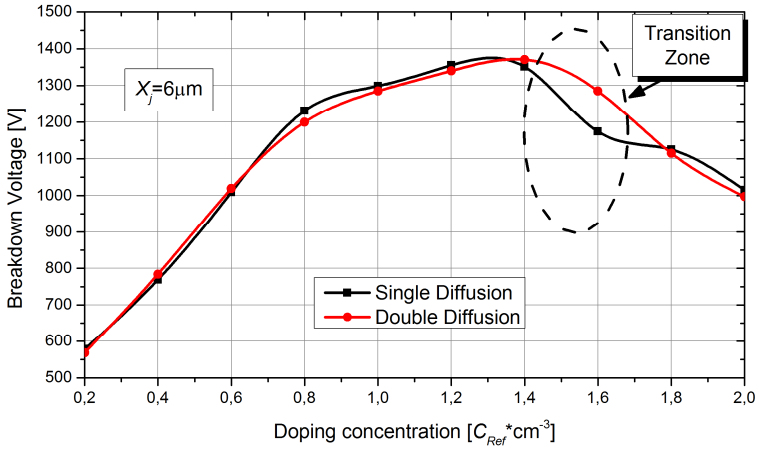


Multi-mask approach

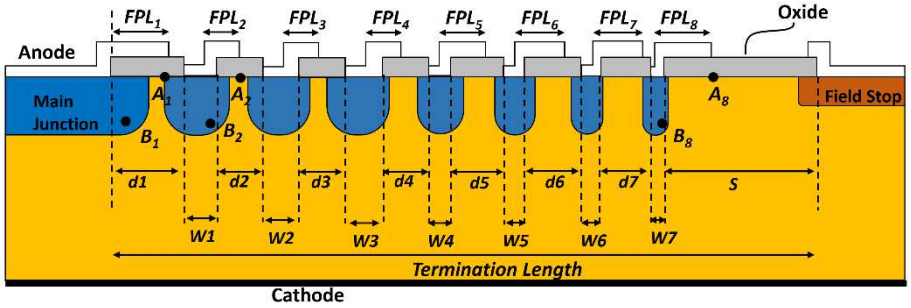


Citation

BV Vs JTE Doping Concentration



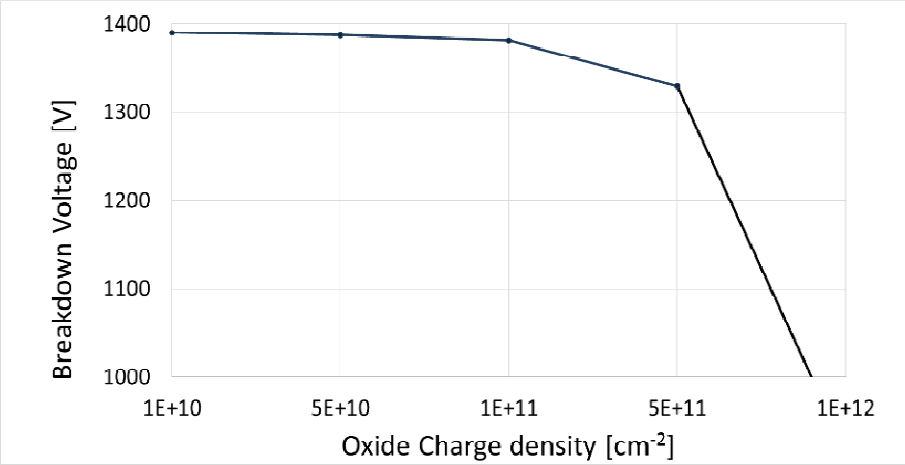
Field Plate assisted FFR Termination



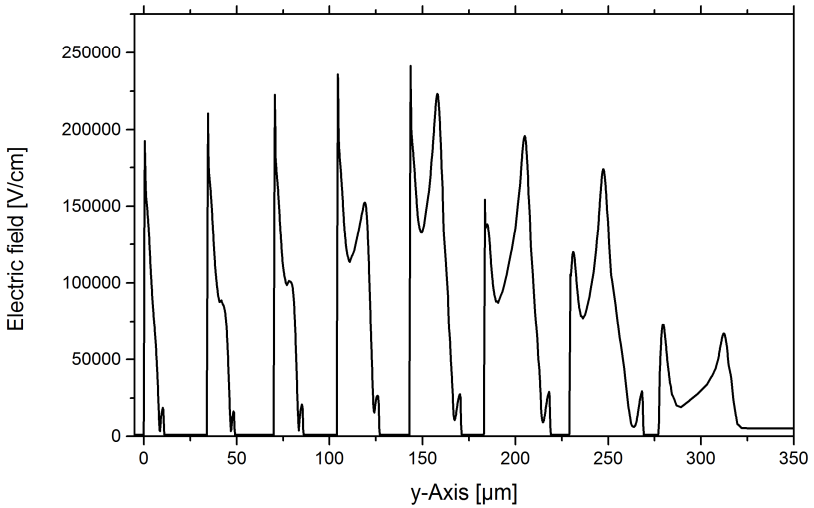
List of Parameters

Parameter	*Symbol*
Distance between Rings	d_n
Ring width	W_n
Filed Plate Lengths	FPL_n

BV Vs Oxide Charge density



Superficial Electric Field distribution



Results comparison

Design	*Length* [µm]	*Xj* [µm]	*Oxide charge rejection*	*BV* [V]
FFR	500	6	↗	1358
FFR	500	8	↗	1401
SIPOS-JTE	250	6	↑	1328
SIPOS-JTE	250	8	↑	1332
SIPOS-JTE	300	6	↑	1381
SIPOS-JTE	300	8	↑	1359
OGA-JTE	400	6	→	1371
OGA-JTE	400	8	→	1360

SIPOS- JTE Termination

Advantages:

- **250 µm** of *Saved* area
- **Great** immunity against impurities and Process fluctuation

Criticalities:

- Resistivity control of SIPOS layer
- Oxide dimensioning

OGA- JTE Termination

Advantages:

- **150 µm** of *Saved* area
- **Good** immunity against impurities and Process fluctuation

Criticalities:

- Mask managing of the Outer Guard-Rings

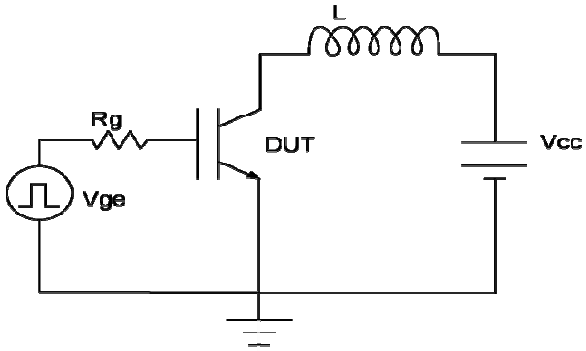
Specific Activity

New Termination Design:

- SIPOS-JTE structure
- OGA-JTE structure

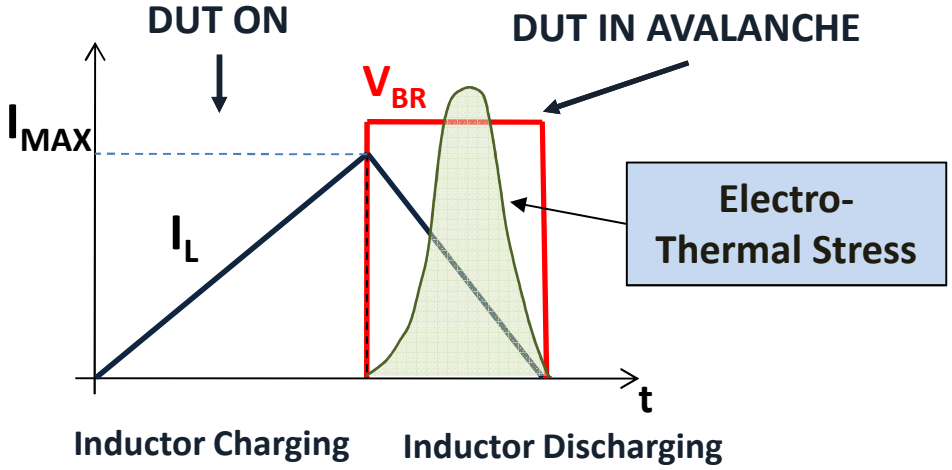
Ruggedness analysis by means of UIS simulations

Ruggedness: UIS Simulations



Avalanche Application: **Unclamped Inductive Switching Test (UIS)** is the standard test for evaluation of devices capability in avalanche operations [JEDEC standards N. JESD24- 5]

Rugged is evaluated considering the **thermal energy** absorbed during the UIS transitory until the **failure condition** (reaching of **700K**)



$$E = \frac{1}{2} L I_{MAX}^2 \frac{V_{BR}}{V_{BR} - V_{CC}}$$

During the **turn-on**:

$$\frac{di_C}{dt} = \frac{V_{DD}}{L} \Rightarrow I_{C,\max} = \frac{V_{DD}}{L} T_{ON}$$

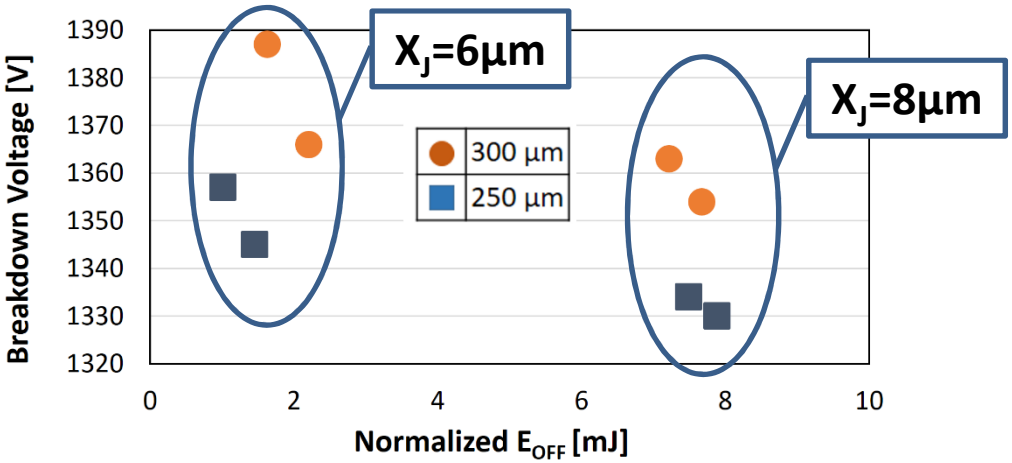
During the **turn-off**:

$$\frac{di_C}{dt} = -\frac{V_{BR} - V_{DD}}{L} \Rightarrow T_{OFF} = \frac{L I_{C,\max}}{V_{BR} - V_{DD}}$$

SIPOS-JTE: UIS Simulations

Anode Peak [cm^{-3}]	Terminanation Length [µm]	X_j [µm]	Ipeak = 10A			Ipeak = 25A		
			L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]	L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]
1x10^{16}	250	6	8,5	7,7	7,5	0,65	0,64	0,64
		8	7,2	6,5	6,5	0,65	0,65	0,65
	300	6	5,2	4,8	4,8	0,7	0,7	0,7
		8	13,1	10,8	10,7	0,7	0,7	0,7
1x10^{17}	250	6	53,4	49,7	49,7	39,5	39,4	39,5
		8	59,3*	55,8	55,9	41,3	41,8	41,9
	300	6	3,8	3,1	3,8	5,8	5,9	5,9
		8	59,6*	57,3	57,5	37,6	37,6	37,5

* Failure condition NOT occurred



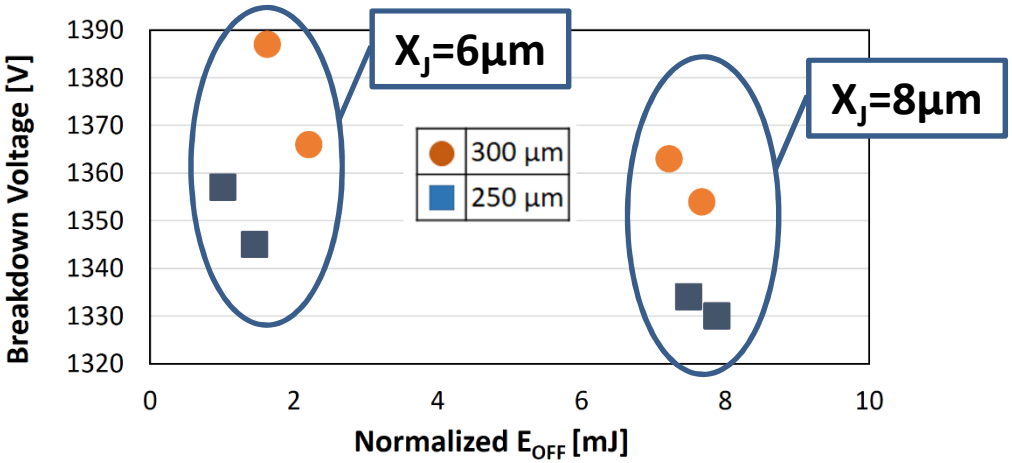
SIPOS-JTE: UIS Simulations

Anode Peak [cm^{-3}]	Terminanation Length [µm]	X_j [µm]	Ipeak = 10A			Ipeak = 25A		
			L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]	L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]
1x10^{16}	250	6	8,5	7,7	7,5	0,65	0,64	0,64
		8	7,2	6,5	6,5	0,65	0,65	0,65
	300	6	5,2	4,8	4,8	0,7	0,7	0,7
		8	13,1	10,8	10,7	0,7	0,7	0,7
1x10^{17}	250	6	53,4	49,7	49,7	39,5	39,4	39,5
		8	59,3*	55,8	55,9	41,3	41,8	41,9
	300	6	3,8	3,1	3,8	5,8	5,9	5,9
		8	59,6*	57,3	57,5	37,6	37,6	37,5

* Failure condition NOT occurred

Current crowding

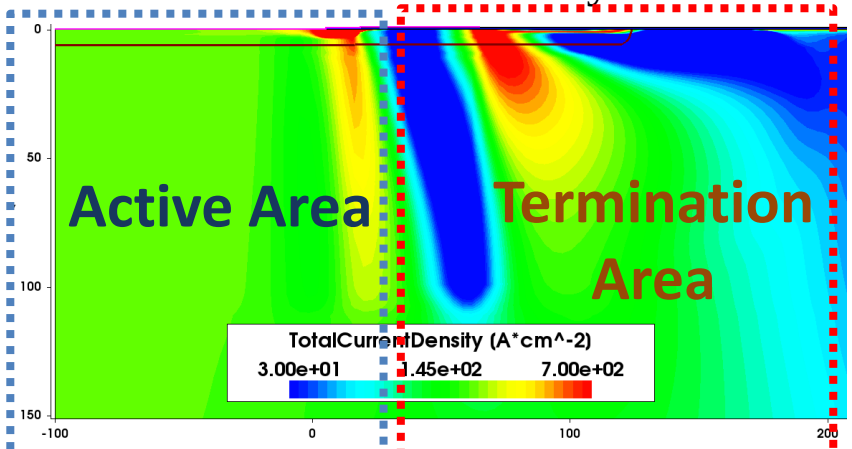
Reach-Through Phenomenon



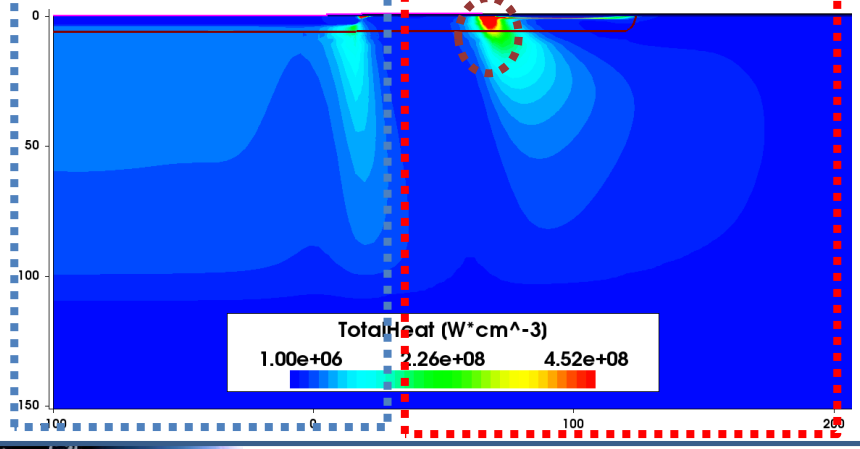
SIPOS-JTE: UIS Simulations

FPL= 45µm, E_{OFF} = **15,4 mJ**

Total current density

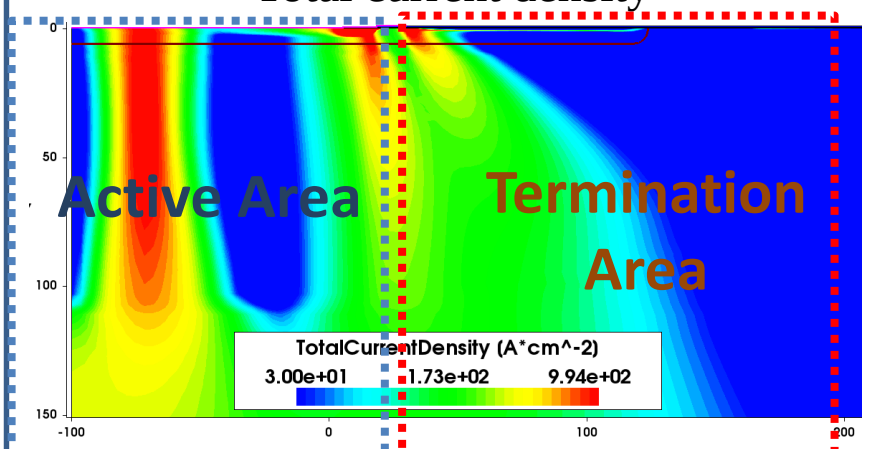


Power distribution

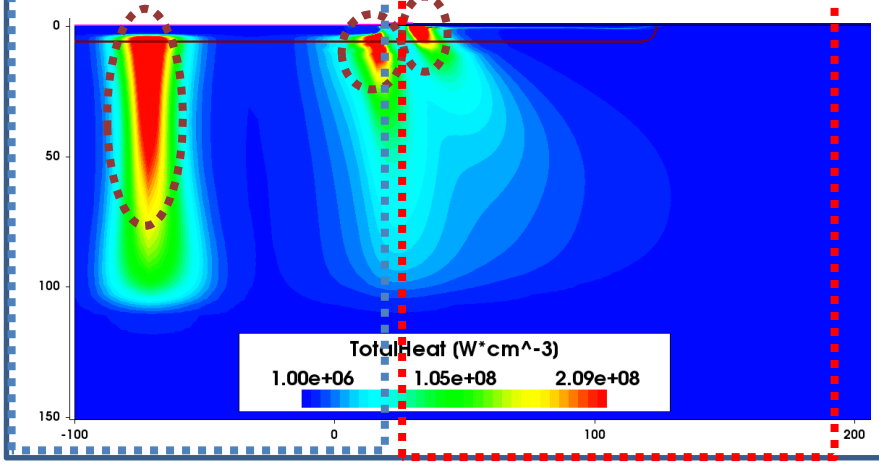


FPL= 15µm, E_{OFF} = **36,9 mJ**

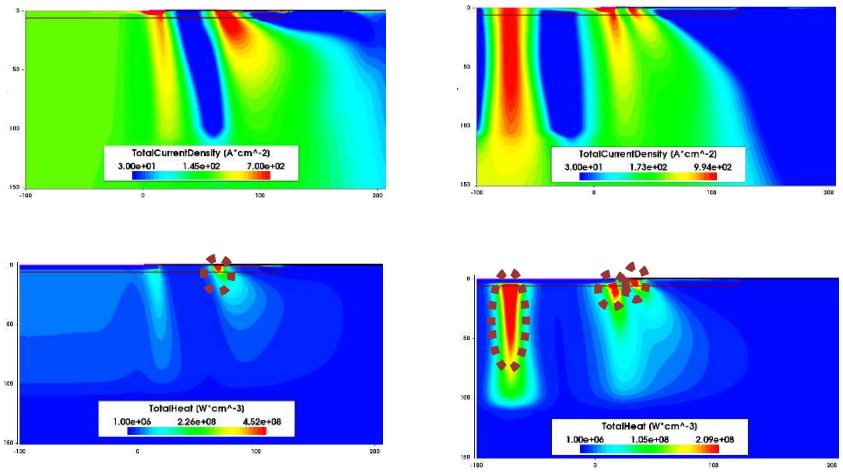
Total current density



Power distribution



SIPIS-JTE: UIS Simulations



The solution adopted has led to a considerable increment of the ruggedness.

A reduced FPL implies a lowering of about 30V of the Breakdown capability.

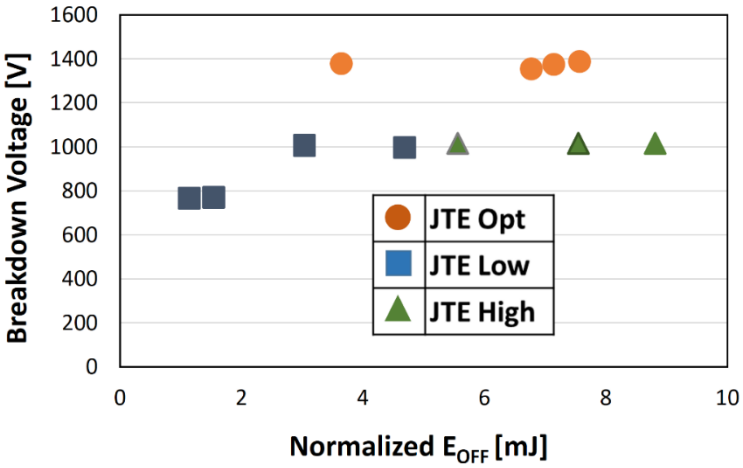
	Anode Peak [cm-3]	Terminanation Length [µm]	Xj [µm]	Ipeak = 10A			Ipeak = 25A		
				L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]	L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]
NEW	$1x10^{17}$	300	6	60,5*	52,9	52,8	41,5	41,8	41,8
OLD	$1x10^{17}$	300	6	3,8	3,1	3,8	5,8	5,9	5,9

OGA-JTE: UIS Simulations

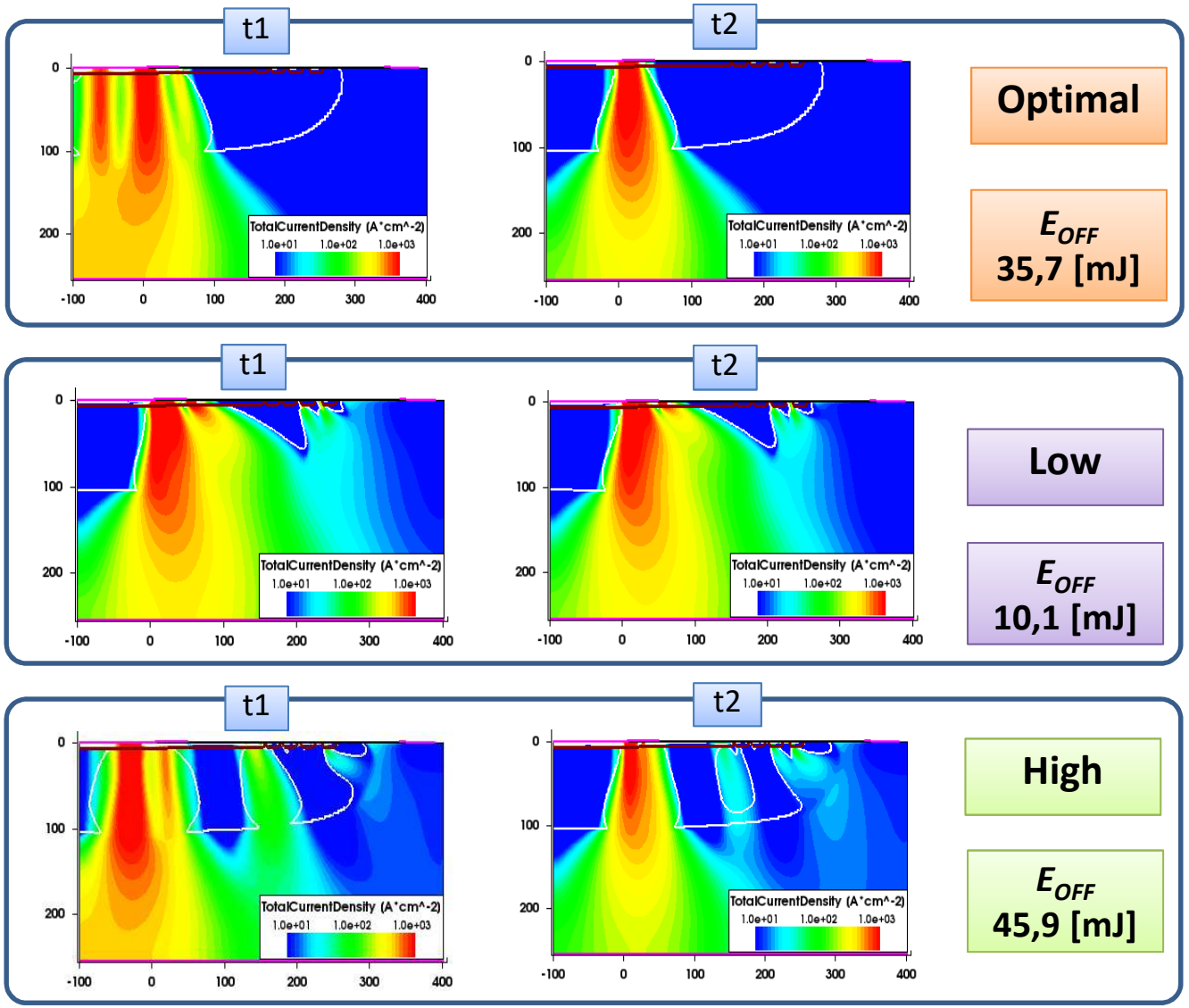
Anode Peak [cm^{-3}]	JTE Peak [cm^{-3}]	X_j [µm]	Ipeak = 10A		Ipeak = 25A	
			L = 1mH	L = 100mH	L = 1mH	L = 100mH
$1x10^{16}$	$6x10^{15}$	6	En = **35,7** [mJ]	En = **31,0** [mJ]	En = **4,5** [mJ]	En = **4,5** [mJ]
	$5x10^{15}$	8	En = **44,9** [mJ]	En = **42,1** [mJ]	En = **34,7** [mJ]	En = **35,7** [mJ]
$1x10^{17}$	$6x10^{15}$	6	En = **43,6** [mJ]	En = **49,8** [mJ]	En = **45,6** [mJ]	En = **47,4** [mJ]
	$5x10^{15}$	8	En = **52,8** [mJ]	En = **51,6** [mJ]	En = **54,0** [mJ]	En = **44,2** [mJ]
$1x10^{16}$	$2x10^{15}$	6	En = **10,1** [mJ]	En = **9,1** [mJ]	En = **4,5** [mJ]	En = **4,5** [mJ]
	$2x10^{15}$	8	En = **27,7** [mJ]	En = **22,1** [mJ]	En = **48,2** [mJ]	En = **47,8** [mJ]
$1x10^{17}$	$2x10^{15}$	6	En = **8,8** [mJ]	En = **8,6** [mJ]	En = **14,7** [mJ]	En = **14,8** [mJ]
	$2x10^{15}$	8	En = **18,7** [mJ]	En = **19,0** [mJ]	En = **25,4** [mJ]	En = **25,6** [mJ]
$1x10^{16}$	$1x10^{16}$	6	En = **45,9** [mJ]	En = **39,9** [mJ]	En = **29,3** [mJ]	En = **29,9** [mJ]
	$1x10^{16}$	8	En = **62,9*** [mJ]	En = **49,3** [mJ]	En = **44,4** [mJ]	En = **44,9** [mJ]
$1x10^{17}$	$1x10^{16}$	6	En = **59,3** [mJ]	En = **60,4** [mJ]	En = **29,8** [mJ]	En = **37,3** [mJ]
	$1x10^{16}$	8	En = **63,3*** [mJ]	En = **68,1** [mJ]	En = **50,7** [mJ]	En = **51,9** [mJ]

Current crowding

* Failure condition NOT occurred



OGA-JTE: UIS Simulations



The design must favor the generation of current paths in active area to increase E_{OFF}.

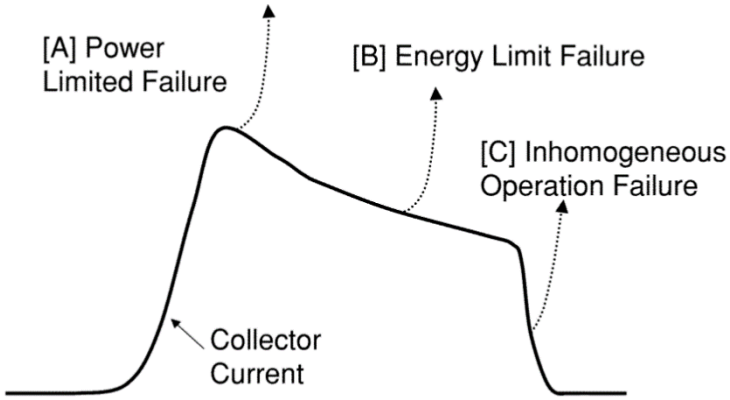
In every cases the failure is caused by the current crowding at the edge of the main junction.

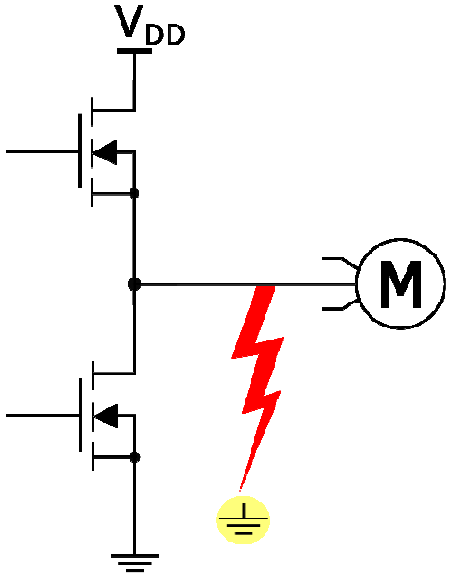
Specific Activity

Short-Circuit capability analysis of the Active Area

Short-Circuit capability analysis

- Standard test used to "evaluate" ruggedness of Power devices, in terms of energy/thermal limits
- Usual requirement for Silicon: **10µs** SC pulse with **2/3 V_{MAX}**





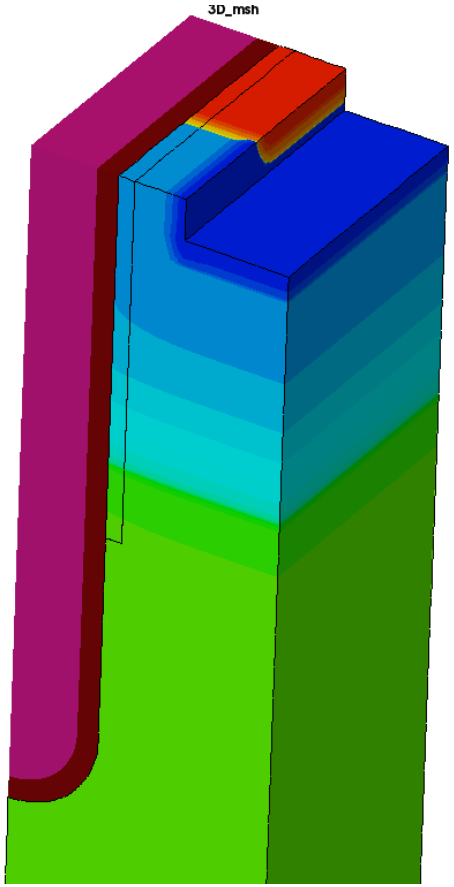
[A] The failure occurs near the peak current[1]
[B] The failure occurs during the steady state due to the high energy dissipation which produces a local increase of temperature[2]
[C] The device fails at the turn-off[3]

[1]T. Wikstorm, et Al, "Experimental study on plasma engineering in 6500 V IGBTs," in *Proc. ISPSD'00*

[2]J. Yamashita et Al, "A study on the short-circuit destruction of IGBTs," in *Proc. 5th ISPSD*

[3]Yamashita, et Al., "A study on the IGBTs turn-off failure and inhomogeneous operation," in *Proc. ISPSD'94*

Emitter Modulation



Short-Circuit capability is strictly related to the Saturation current

Saturation current can be reduced adopting the modulation of the Emitter diffusion region (N^+)[1,2]

The Emitter modulation can be defined as the ratio between N^+-Emitter diffusion length along the z-axis and the elementary cell length along the z-axis expressed in percentage

Design	V_{on} [V] at J_C = 100A/cm²	I_{SAT} [A] at V_{CE} = 10V
M 25	1.429	17.3
M 50	1.288	28.7
M 75	1.244	39.4

1. H. Yilmaz, "Cell geometry effect on IGT latch-up," in *IEEE Electron Device Letters*
2. Chong Man Yun, et Al., "Comparison of stripe and cellular geometry for short circuit rated trench IGBT," *12th ISPSD*

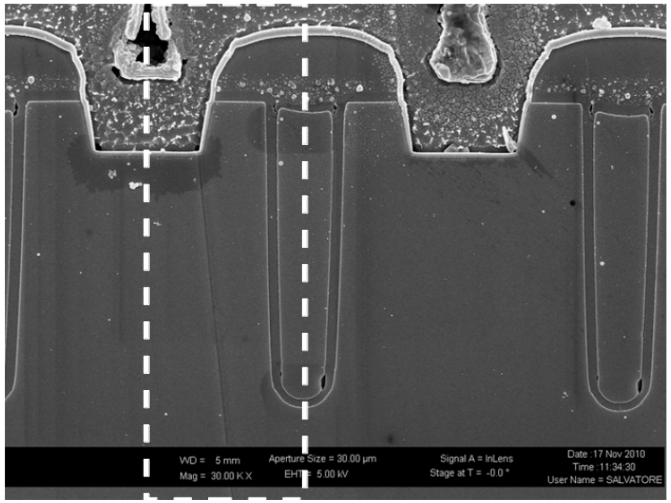
Specific Activity

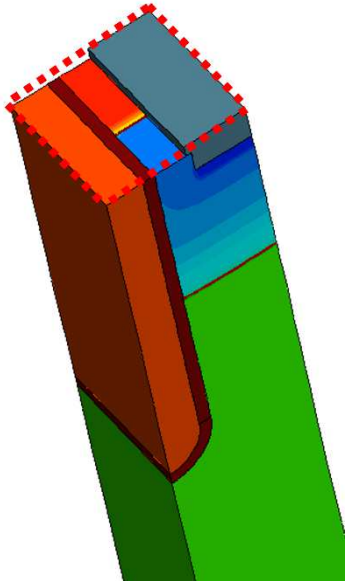
Short-Circuit capability analysis of the Active Area

Calibration of a 3D elementary cell of a commercial FS-IGBT device

Elementary cell Calibration

SEM image

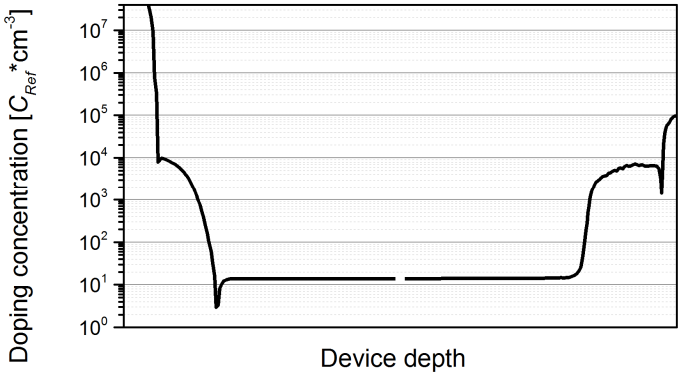




Measurements setup:

- Curve tracing
- ILS test for calculation of Lifetime dependence on temperature
- Short-Circuit test

Vertical Doping Profile



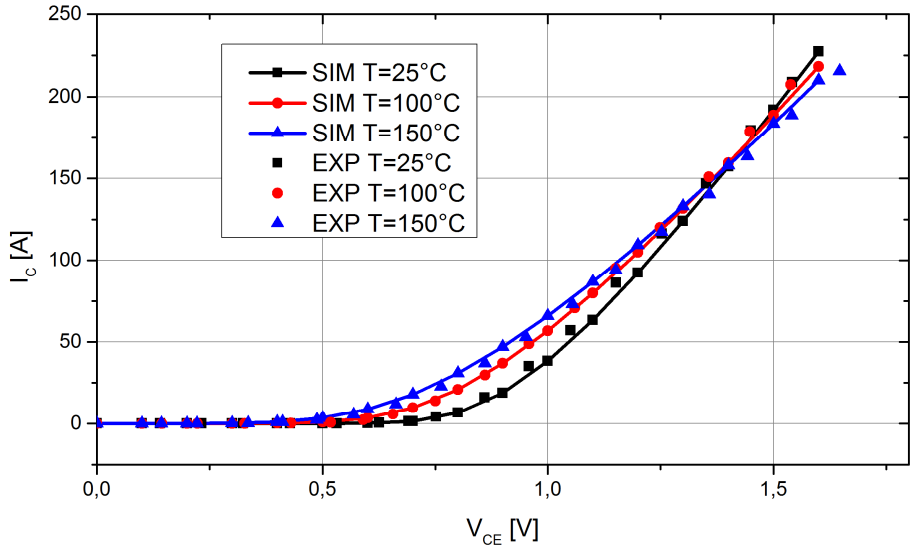
Physical models calibration

Model	*Symbol*	*Default Value*	*Calibrated Value*
Scharfetter	τ_n	$1x10^{-5}$ [s]	$6.921x10^{-7}$ [s]
	τ_p	$3x10^{-6}$ [s]	$2.078x10^{-7}$ [s]
	N_{Ref}	$1x10^{16}$ [cm^{-3}]	$8x10^{15}$ [cm^{-3}]
	T_α	-1.5	3.5
	E_{trap}	0.33 [eV]	-0.2 [eV]
Arora	$\mu_{max,n}$	1252 [cm^2/V·s]	1001.6 [cm^2/V·s]
	$\mu_{min,n}$	88 [cm^2/V·s]	70.4 [cm^2/V·s]

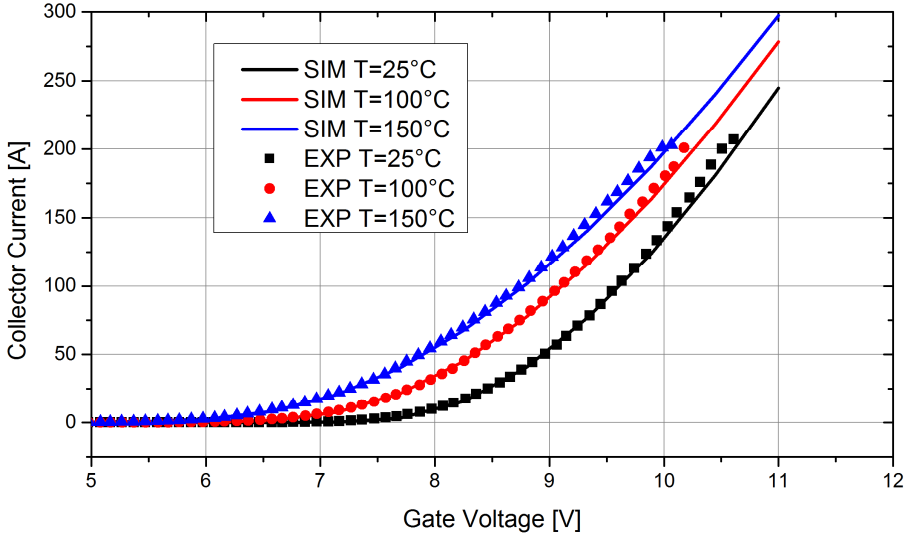
Calibration results

- Experimental and simulation characteristic are achieved at different temperature
- Results show a good fitting of the simulated curves

I_C-V_{CE} Characteristics



I_C-V_{GE} Characteristics



Specific Activity

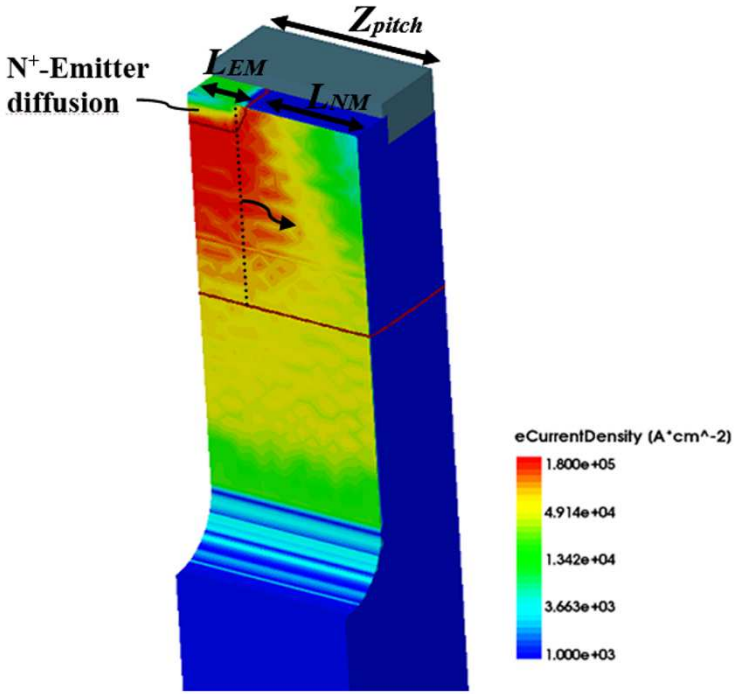
Short-Circuit capability analysis of the Active Area

Proposal of new Design able to increase the Short-Circuit capability

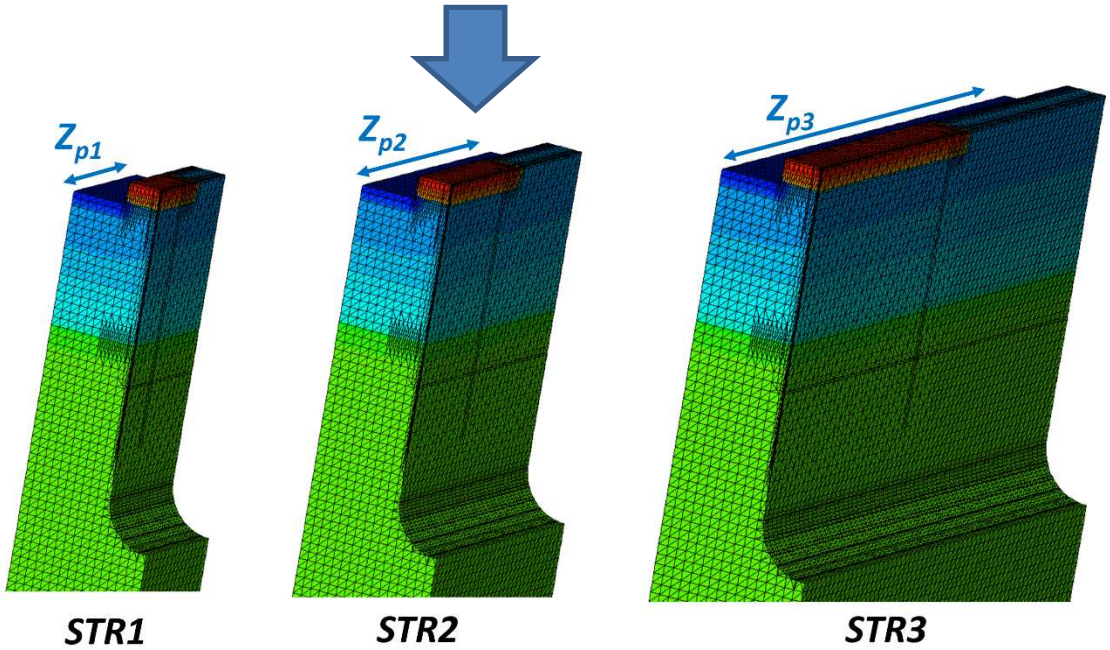
Design Proposal

The carriers lateral spread is limited by the lifetime:

$$L_D = \sqrt{\tau D}$$



The effect of the ***Transversal Cell Pitch*** (*Zp*) is evaluated for a fixed Emitter Modulation



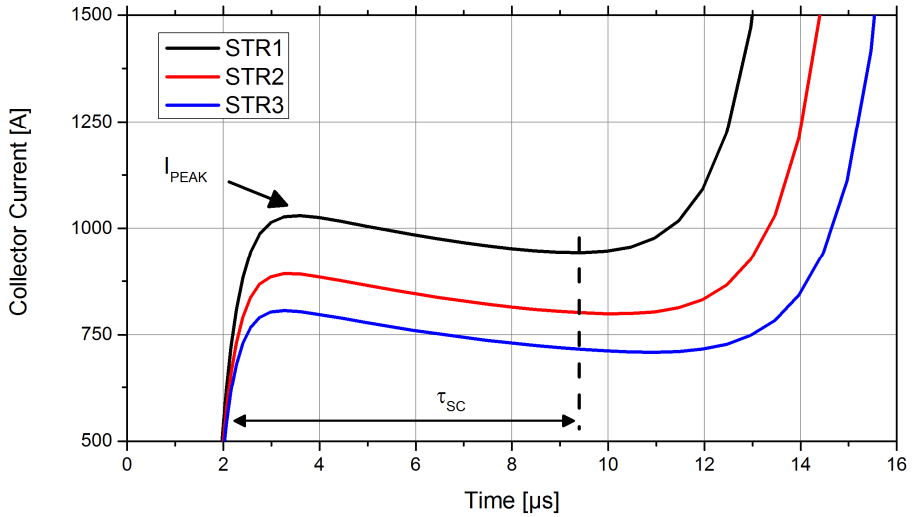
Z_{p1}: 0.5·Z_{p2}: 0.25·Z_{p3}.

Simulation results of the proposed design

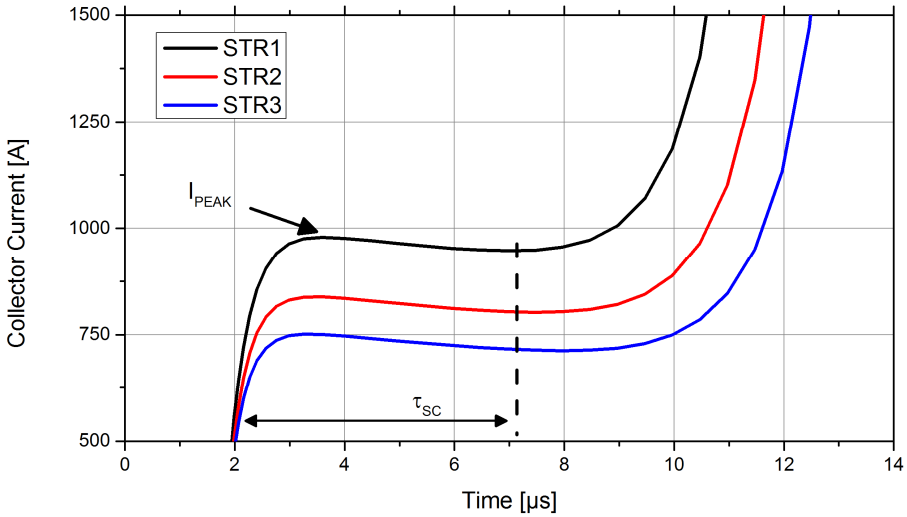
Design	*Ipeak* [A] at T=25°C at T=150°C	V_{ON} [V] (at 200A) at T=25°C at T=150°C	τ_{SC} [µs] at T=25°C at T=150°C
STR1	1030 979	1.515 1.557	7.8 5.3
STR2	892 838	1.552 1.608	8.5 5.8
STR3	806 750	1.601 1.682	8.7 6.3

The Salutation current reduces with increasing the *Transversal Cell Pitch*, resulting in a Short-Circuit capability increase.

T = 25°C



T = 150°C

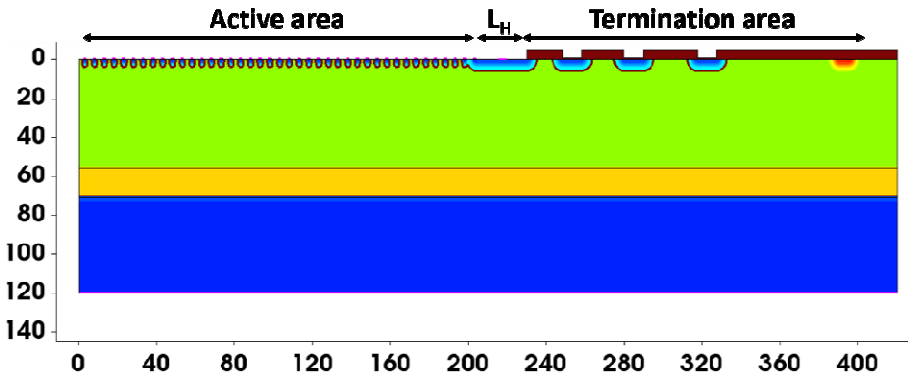


Specific Activity

Other Activities

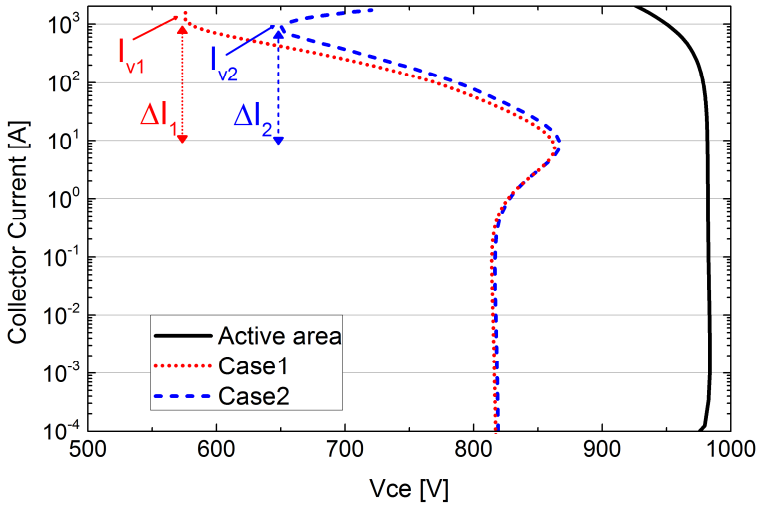
- Current crowding phenomenon
- Emulation of Termination fabrication process
- Study and analysis of RC-IGBT devices

NDR relation with filamentation



Filamentation is a 3D effect

$$A_{Filament} = I_{Force} / J_{Valley}$$



In 2D analysis the transversal dimension has been set proportional to the Filament Area

Simulations confirm the Experimental results

Lower ΔI allows to increase the failure time, hence, turn-off energy capability

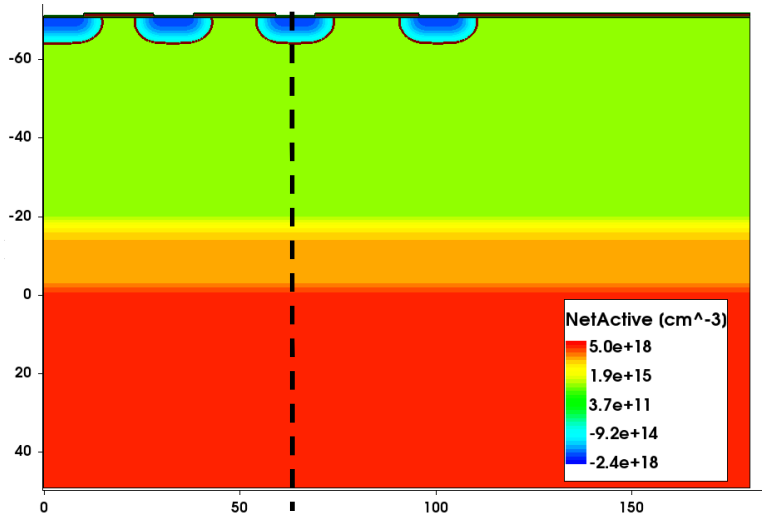
Emulation of a FFR technological process

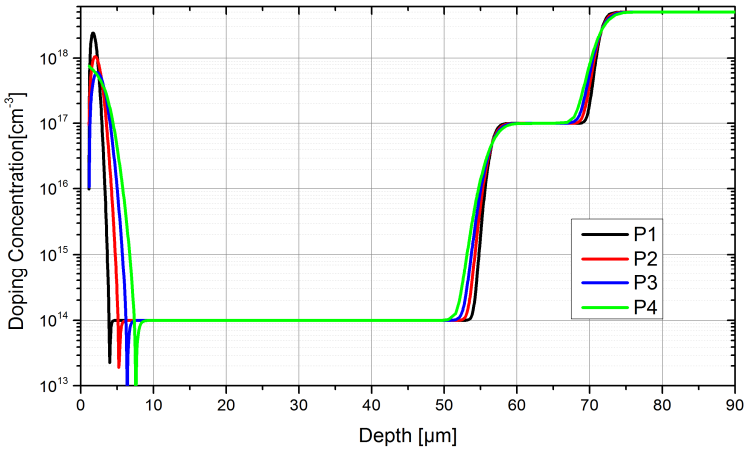
Sentaurus PROCESS tool

Termination FFR 600V for Punch-Through IGBT

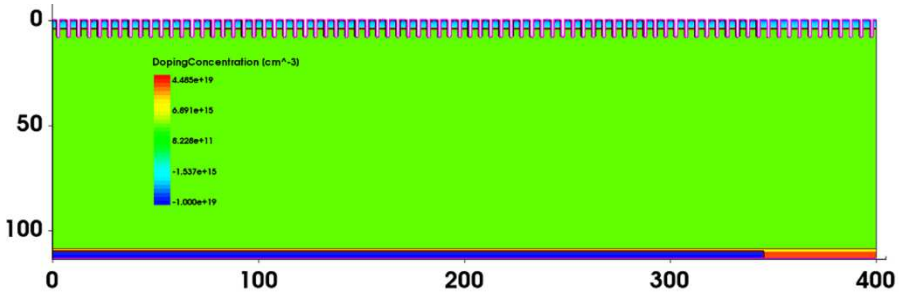
The process flow consists in the following steps:

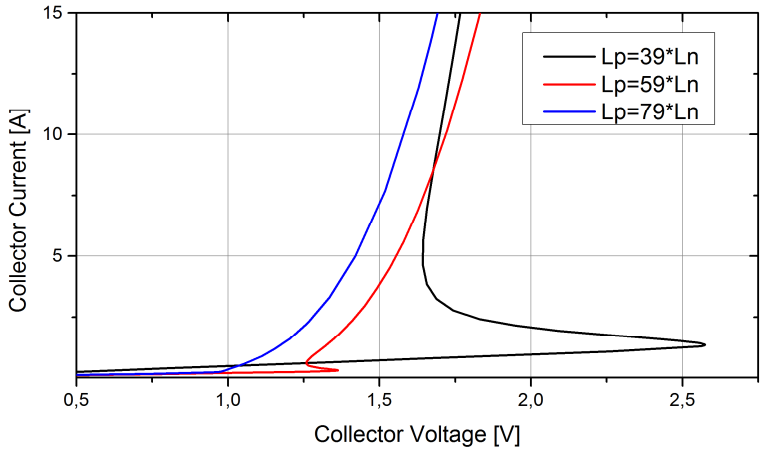
- Epitaxial growing
- Oxide growing on the epitaxial layer
- Boron implantation and diffusion
- Trench Gate generation process
- Active area implantations and diffusions





Reverse Conducting (RC)-IGBT





- Study of the state-of-art design.
- Analysis of the Snap-back phenomenon correlated to the Buffer layer dimension and doping.
- Analysis of the carrier distribution during the transitory. Adoption of Lifetime Killing techniques.

$$V_{Snap-Back} = \frac{LI_0}{Zq\mu_n N_D (L_p + L_n)}$$

Credit Summary

	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	6			3		3		6	15		6				9	15	9						9	9	30	30-70
Seminars	5,1	0,2	1		2,8	0,5	0,6	5,1	5,2	1,2				2,4	1,6	5,2	0							0	10	10-30
Research	35	8	9	6	6	5	1	35	38	7	6	6	9	5	5	38	76	13	13	13	12	10	6	67	140	80-140
	46	8,2	10	9	8,8	8,5	1,6	46	58	8,2	12	6	9	7,4	16	58	85	13	13	13	12	10	15	76	180	180

Training abroad: Three moths period to the Fraunhofer Institute (ISIT) in Germany. Main activities were focused on Fabrication Process of Semiconductor Power devices.

Published/being published works

- P.Mirone, et Al, "*Area-Effective JTE-Based Terminations for 1.2 kV Power Diodes*" submitted to *Microelectronic Reliability*.
- L. Maresca, et Al, "*Physics of Current Limited Failures During Avalanche for 600V Fast Recovery Diodes*", accepted to *ISPSD 2017*.
- M. Riccio, et Al., "Accurate SPICE modeling of Reverse Conducting IGBTs including self-heating effect," *in IEEE Transactions on Power Electronics* , vol.PP, no.99, pp.1-1
- M. Riccio *et al.*, "An electro-thermal SPICE model for Reverse Conducting IGBT: Simulation and experimental validation," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Prague, 2016, pp. 343-346.
- A. Irace, et Al., "200 V Fast Recovery Epitaxial Diode with superior ESD capability", *Microelectronics Reliability, Volume 64*, September 2016, Pages 440-446
- P. Mirone, et Al., "On the avalanche ruggedness of optimized termination structure for 600 V punch-through IGBTs*", Microelectronics Reliability*, 6 Dec. 2015
- Mirone, P.; et Al., "A comprehensive study of current conduction during breakdown of Floating Field Ring terminations at arbitrary current levels," in *PCIM Europe 2015*; Proceedings of , vol., no., pp.1-8, 19-20 May 2015
- Mirone, P.; et Al., "An area-effective termination technique for PT-Trench IGBTs," *in Microelectronics Proceedings - MIEL 2014, 29th Int. Conf.* on , pp.273-276, 12-14, May 2014

Attended courses and seminars

Courses:

- Meccanica Quantistica - Prof. Miano
- Europrogettazione - Dr. Varchetta
- English Language Course - Prof. Thomas
- Integrated Photonics – Prof. Breglio
- System on Chip – Prof. Petra

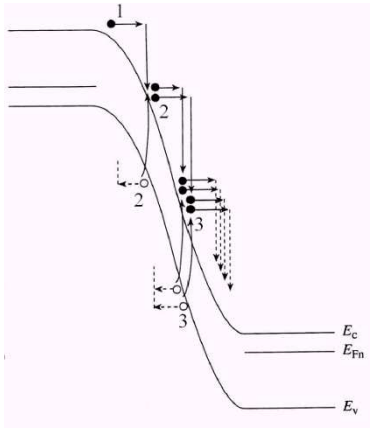
Seminars:

- Quantum Teleportation - Prof. Miano
- Novel tendencies in power devices and circuits - Prof. Castellazzi A
- High dimensional pattern recognition - Prof. Sansone
- Fractional programming for energy efficiency in wireless networks - Prof. De Maio
- Nano-carbon based components and materials for high frequency electronics -- Prof. Miano
- Circuiti quantistici – Prof. Miano
- Towards agile flight of vision-controlled micro flying robots: from frame-based to event-based vision - Prof. Siciliano
- Site reliability engineering at google - Prof. Tramonatana
- Reliability and availability modeling in practice - Prof. Cotroneo
- Capacity planning for infrastructure as a service cloud - Prof. Cotroneo
- Efficient service distribution in next generation cloud networks - Prof. Tulino
- Affidabilità di dispositivi e moduli elettronici di potenza – Prof. Irace
- Test and diagnosis of integrated circuits – Prof. Casola
- Gallium Nitride for power applications: benefits, challenges, and state of the art – Prof. Napoli
- Analisi di segnali a banda larga mediante l'utilizzo di strumentazione Tektronix

- THANK YOU

Breakdown phenomenon

PN junction



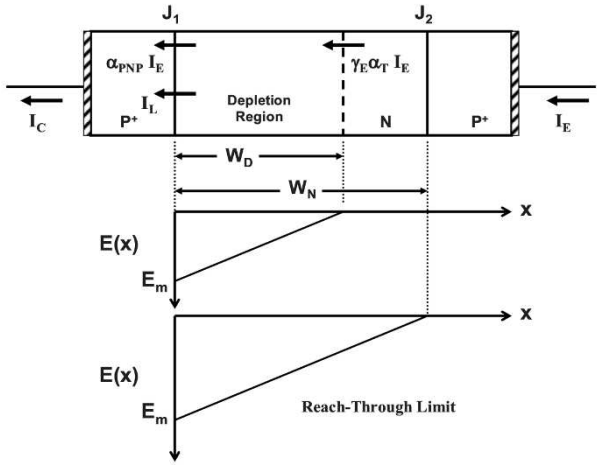
The device Voltage is limited by Avalanche Breakdown. It is a multiplication phenomenon of carriers depending on the Electric Field distribution within the semiconductor.

$$M(x) = 1 + \int_0^x \alpha_n M(x)dx + \int_x^W \alpha_p M(x)dx$$

$$I = M \cdot I_0$$

where M is the avalanche Multiplication coefficient and W is the deplation region width.

PNP junction

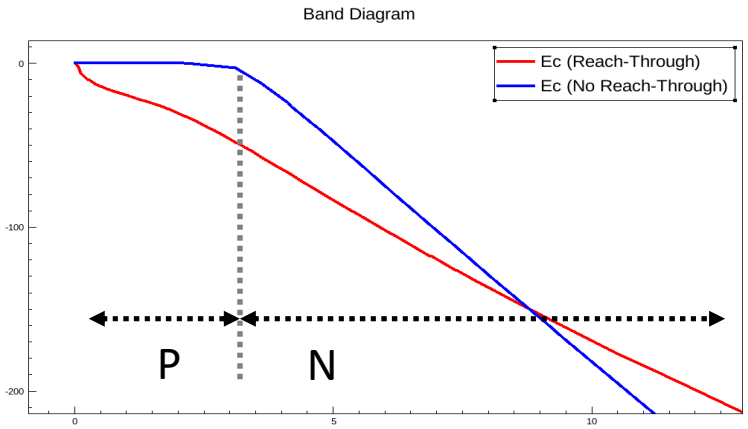


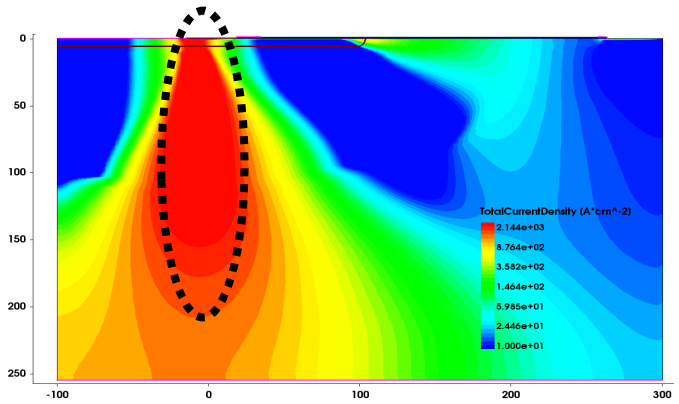
In PNP junctions

$$I_{CB0} = \frac{M \cdot I_{CB0}}{1 - \alpha_{PNP} \cdot M}$$

where ALPHA in the gain of the PNP structure

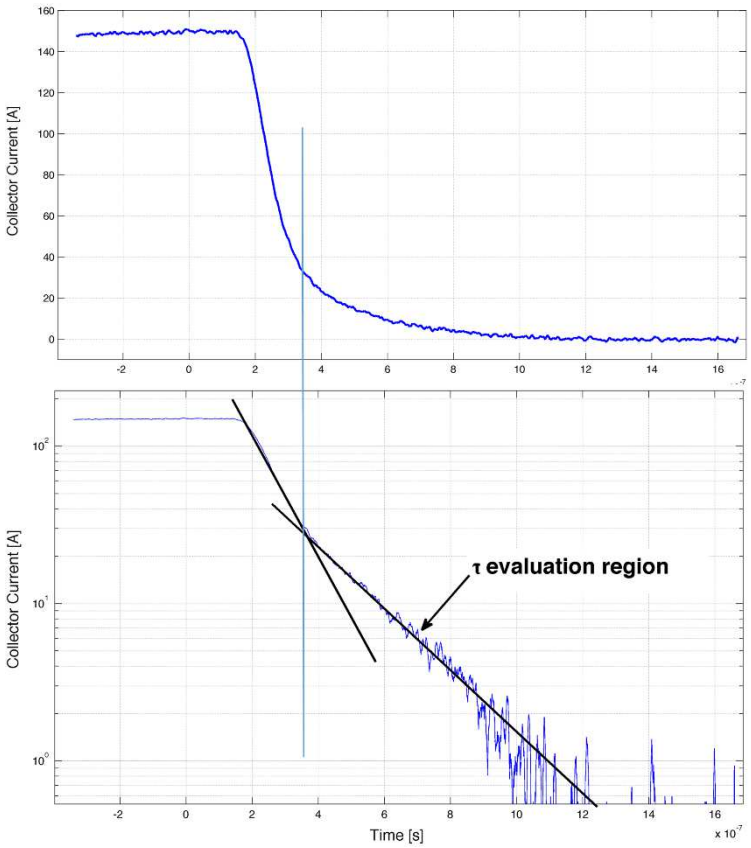
Reach-Through during UIS simulations



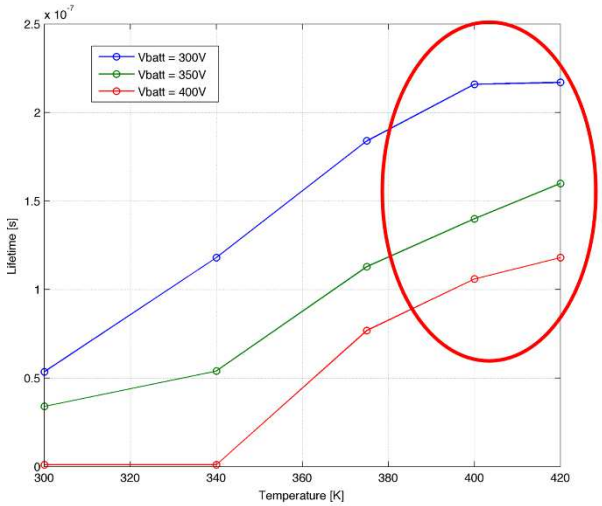


FS-IGBT: Experimental Measurements

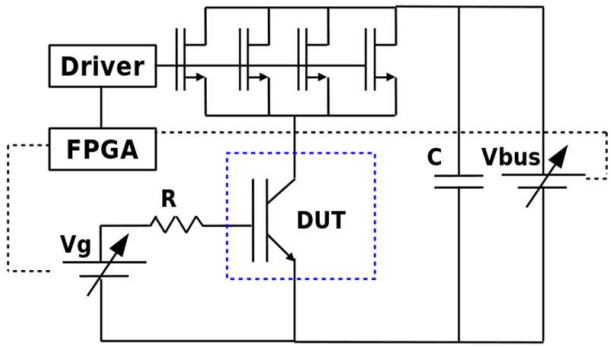
ILS waveforms



Extrapolated Lifetime Vs Temperature



Experimental set-up of the pulsed curve-tracer



Experimental and simulation comparison