PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Paolo Mirone

XXIX Cycle

Training and Research Activities Report – Third Year

Tutor: Prof. Andrea Irace

1. Information

Paolo Mirone received B.S. (2010) and M.S. (2013) degrees in Electronic Engineering from the University of Naples "Federico II". He is currently PhD Student with the Department of Electrical Engineering and Information technologies (DIETI) at University of Naples "Federico II". His tutor is the Assoc. Prof. Andrea Irace. His research interests include modeling, simulation and experimental characterization of semiconductor power devices.

2. Study and Training activities

The second year activities are reported in the following table:

Summary	
Activity	**Credits**
Modules	9
Seminars	0
Research	68

Didactic Activity		
Course Title	**Given by**	**Credits**
System on Chip	Prof. N. Petra	9

Conference papers		
Title of work	**Conference**	**Date**
An electro-thermal SPICE model for Reverse Conducting IGBT: Simulation and experimental validation	IEEE, ISPSD 2016	14-19 Luglio

Journal papers	
Title of work	**Published by**
200 V Fast Recovery Epitaxial Diode with superior ESD capability	Elsevier Editorial System(tm) for Microelectronics Reliability
Accurate SPICE modeling of Reverse Conducting IGBTs including self-heating effect	*IEEE Transactions on Power Electronics*

Seminars	
Seminar Title	**Organized by**

3. Research activity

Third year of research

My activity research are in the field of power electronic devices. They operate in power conversion system as power switches able to impose the ON/OFF condition. A power device present two macroscopic areas: 1) active area; 2) termination area. The first one is responsible of conduction during the On-state of the device; while the second one mainly contributes to withstand the voltage rate during the Off-state condition. The actual trend of power devices tends to a technological scaling to increase the switching frequency and reduce the costs. As consequence, the percentage of the die area occupied by the termination is even more growing since its dimension is related to the voltage rate. This introduce the necessity to develop new termination design able to sustain the same voltage rate with a reduced consumption of area. At the same time, the new designs must also guarantee the required standard in term of reliability and ruggedness consolidated in classical designs. The scaling has also effects on the active area, where current density is even more growing leading to reliability problem from the thermal point of view. The design of new termination structure, as well as, reliability analysis of the active area have been the main focus of my third year research activities.

Two new termination structure have been designed by means of 2D TCAD simulations. The new design realize an improvement of the classical Junction Termination Extension (JTE) technique to sustain a voltage rate of 1.2 kV. JTE design offers the possibility to considerably reduce the occupation of area but present great limitations in term of reliability. JTE needs of optimizing a low-doped P-region to maximize the breakdown voltage of the device. The critical point is that the breakdown voltage is strongly affected by the doping profile of the low-doped region. The breakdown stability is guaranteed only around the optimal value of the doping concentration. A deviation from the optimal value of about 7-8% already produces an inacceptable degradation of the breakdown capability. Since technological process can be subjected to fluctuation or/and contamination of external impurity able to modify the doping profile have led the JTE design to be less attractive for industry. In my activity two innovative two innovative JTE-based terminations have been presented providing a well precise optimization methodology to maximize the breakdown voltage. Both designs have been developed in order to increase the reliability of the device guaranteeing the breakdown stability in a wide range of doping concentration of the low-doped P-region. The first one design exploits the action of a special passivation layer named SIPOS; while the second one is made combining both JTE and a classical Floating Filed Ring technique. The performances of both terminations are than compared with that an advanced Floating Field Ring structure appropriately optimized. Termination ruggedness has been evaluated by means of Unclamped Inductive Switching simulations as the capacitance of power absorption until the failure event. Therefore, current crowding phenomena occurring in avalanche condition are deeply analyzed together with its relation with the Negative Differential Resistance branch on the I-V avalanche curve.

During the third year I spent three months period to the Franhoufer Institute (ISIT). My research was focused on aspects regarding technological process of power devices. During this period I realized an emulation process flow of a Floating Field Ring termination for a 600V Punch-Through IGBT.

The reliability of the active area was analyzed by means of Short-Circuit test. It is an industrial test able to evaluate the capacitance of power absorption during the Short-Circuit condition of a device. During the Short-Circuit, the device is driven in conduction at high voltage and the current is limited only by the internal resistance. The influence of design parameters on the Short-Circuit capability of a FS-IGBT device has been analyzed. A commercial device has been experimentally characterized by means of static curves tracker, Inductive Load Switching test and Short-Circuit test. The Short-Circuit capability analysis was led with a simulation approach by means of 3D TCAD electro-thermal simulations. The physical models of the elementary cell of the IGBT device have been calibrated to fit the characteristics of the commercial device at different temperatures. An innovative design has been proposed to increase the Short-Circuit capability.

4. Products

Published works:

- A. Irace, et Al., “200 V Fast Recovery Epitaxial Diode with superior ESD capability”, *Microelectronics Reliability, Volume 64*, September 2016, Pages 440-446
- M. Riccio, et Al., "Accurate SPICE modeling of Reverse Conducting IGBTs including self-heating effect," *in IEEE Transactions on Power Electronics* , vol.PP, no.99, pp.1-1

Accepted but not yet published works:

- P. Mirone, et Al, “*Area-Effective JTE-Based Terminations for 1.2 kV Power Diodes*” submitted to *Microelectronic Reliability*.
- L. Maresca, et Al, “*Physics of Current Limited Failures During Avalanche for 600V Fast Recovery Diodes*”, accepted to *ISPSD 2017*.

5. Conferences and Seminars

I participated at a IEEE International Conference:

- M. Riccio et al., "An electro-thermal SPICE model for Reverse Conducting IGBT: Simulation and experimental validation," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 343-346.