PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Paolo Mirone

XXIX Cycle

Training and Research Activities Report – Second Year

Tutor: Prof. Andrea Irace

1. Information

Paolo Mirone received B.S. (2010) and M.S. (2013) degrees in Electronic Engineering from the University of Naples "Federico II". He is currently PhD Student with the Department of Electrical Engineering and Information technologies (DIETI) at University of Naples "Federico II". His tutor is the Assoc. Prof. Andrea Irace. His research interests include modeling, simulation and experimental characterization of semiconductor power devices.

2. Study and Training activities

The second year activities are reported in the following table:

Summary	
Activity	**Credits**
Modules	15
Seminars	5.2
Research	31

Didactic Activity		
Course Title	**Given by**	**Credits**
English Language Courses	Prof. G. Thomas	6
Integrated Photonics	Prof. G. Breglio	9

Conference papers		
Title of work	**Conference**	**Date**
A comprehensive study of current conduction during breakdown of Floating Field Ring terminations at arbitrary current levels	IEEE, PCIM 2015	19-22 Maggio

Journal papers	
Title of work	**Published by**
On the avalanche ruggedness of optimized termination structure for 600V Punch-Through IGBTs	Elsevier Editorial System(tm) for Microelectronics Reliability

Seminars	
Seminar Title	**Organized by**
Cycles of 3 seminars “Affidabilità di dispositivi e moduli elettronici di potenza”	Prof A. Irace
Cycles of 2 seminars “Test and diagnosis of integrated circuits”	Prof.ssa V. Casola
“Gallium Nitride for power applications: benefits, challenges, and state of the art”	Prof. E.Napoli
“Analisi di segnali a banda larga mediante l’utilizzo di strumentazione Tektronix”	

3. Research activity

Second year of research

The aim of my doctoral activity concerns the comprehension, analysis and development of the state-of-art of an RC-IGBT [1]. In particular, I have focused my research activities on structures 600V and 1200V rated. By means of 2D TCAD simulations, I analyzed the problematic of termination robustness in avalanche conditions. Termination effectiveness can be experimentally evaluated with Unclamped Inductive Switching (UIS) test that is commonly used to validate the avalanche robustness of Power devices [2]. What is more, UIS test allows to evaluate the device maximum energy capability before its catastrophic failure. Many papers attribute a lowering of the maximum sustainable energy to the presence of an uneven current distribution (current filamentation) [3]. Such phenomenon produces a local temperature increase that leads to a premature failure of the device. In some papers, it has been investigated the relation between the filamentation current and the Negative Differential Region in the static I-V avalanche characteristic [4]. In this scenario, I used static I-V avalanche curves to address the UIS test in order to analyze electro-thermal instabilities due to the filament occurring in termination region. The core of my activity is then to design different termination solutions to increase either the breakdown voltage capability and to improve the robustness.

I have implemented two type of terminations design: the first one exploits the combined action of an high-resistive layer (SIPOS) and P^- diffusion to modulate the superficial electric field; the second one, called Guard Assisted technique, combines the action of high-doped and low-doped diffusions to improve the instabilities due to the technological process. In both cases, the target is to reduce the overall termination dimension without sacrifice the maximum breakdown voltage and the robustness. Many parameters can be managed to optimize the structure design, each of them subjected to technological constraints. Since each parameter influences the effect of the other, it will be needed to evaluate the best trade-off solutions.

With the first design, I used the SIPOS layer to linearize the superficial electrostatic potential and the fully depleted P^- diffusion to increase the breakdown voltage. This technique leads to high-efficiency performances with a reduced consumption of periphery area. The main issue is the difficulty to realize a high quality SIPOS layer. SIPOS layer must be the higher resistive possible in order to reduce the leakage current contribution. This can be achieved through different doping steps of the polycrystalline structure [5].

The second design is thought to improve the technological limits of the JTE technique. This last essentially consists of P^- diffusion able to sustain great breakdown voltage with a lower consumption of area. Nevertheless, it shows its high efficiency only at well precise doping dose of the P^- diffusion. This is a critical aspect since a real technological process always presents some variation respect to the awaited values. The guard assisted approach allows enlarge the window of doping dose at which the termination works at high performance. It exploits the influences of P^+ diffusion to increase the “window” toward low dose values, and the action of further P- diffusions to increase it toward higher value.

For the third year of doctorate is planned to physically realize these two terminations design, which will allow to pass at a testing phase.

References:

[1] S.Voss, O.Hellmund, W.Frank, “New IGBT concepts for Consumer Power Applications,” IEEE IAS, 2007, New Orleans 2007

[2] G. Breglio, et Al., "Experimental Detection and Numerical Validation of Different Failure Mechanisms in IGBTs During Unclamped Inductive Switching," Electron Devices, IEEE Trans. , vol.60

[3] H.-J. Schulze, F.-J. Niedernostheide, F. Pfirsch, and R. Baburske, “Limiting factors of the safe operating area for power devices,” IEEE Trans.Electron Devices, vol. 60, no. 2, pp. 551–562, Feb. 2013.

[4] Spirito, P.; Maresca, L.; Riccio, M.; Breglio, G.; Irace, A.; Napoli, E., "Effect of the Collector Design on the IGBT Avalanche Ruggedness: A Comparative Analysis Between Punch-Through and Field-Stop Devices," in Electron Devices, IEEE Transactions on , vol.62, no.8, pp.2535-2541, Aug. 2015

[5] T. Matsushita et al., “Highly reliable high-voltage transistors by use of the SIPOS process”, IEEE Trans. Electron Devices, vol. ED- 23, pp. 826–830, Aug. 1976.

4. Products

Published works:

- P. Mirone et al., "*A comprehensive study of current conduction during breakdown of Floating Field Ring terminations at arbitrary current levels*," PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, Nuremberg, Germany, 2015,
- Paolo Mirone, Luca Maresca, Michele Riccio, Giovanni Breglio, Andrea Irace, “*On the avalanche ruggedness of optimized termination structure for 600 V punch-through IGBTs*”, Microelectronics Reliability, Available online 6 December 2015

Accepted but not yet published works:

- M. Riccio, M. Tedesco, P. Mirone, G. De Falco, L. Maresca, G. Breglio and A. Irace, “*An electro-thermal SPICE model for Reverse Conducting IGBT: simulation and experimental validation*”, ISPSD Conference.

For the third year, it is in program a research period at the Frounhofer Institute of Itzehoe (Germany). It will regard activities on IGBTs power devices.

5. Conferences and Seminars

I participated as Poster presenter at IEEE International Conference:

PCIM Europe 2015, Nuremberg (Germany), 19-22 May 2015, "A comprehensive study of current conduction during breakdown of Floating Field Ring terminations at arbitrary current levels"