PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Ilaria Matacena

XXXIII Cycle

Training and Research Activities Report – Third Year

Tutor: Santolo Daliento

1. Information
   I received the M. Sc. Degree in Electronic Engineering from University of Napoli 'Federico II' in December 2016. I belong to XXXIII cycle of Information Technology and Electrical Engineering (ITEE) PhD. My fellowship is financed by athenaeum. My tutor is Prof. Santolo Daliento.

2. Study and Training activities
   During this second year I followed some IEEE modules to widen my knowledge.
   Study and training activities are summarized below:

   a. External courses (IEEE courses):
      i. "Grid Modernization: Smart Distribution Systems from Power and Energy" (0.3)
      ii. "An Introduction to Sustainable Green Engineering: Part 1" (0.3)
      iii. "An Introduction to Sustainable Green Engineering: Part 2" (0.3)
      iv. "Introduction to Sustainable Green Engineering System Analysis and Design" (0.3)
      v. "Applications of Finite Element Method: Modelling of multilayer stacks/anti-reflection coatings" (0.3)

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Cycle XXXIII

	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0	0	4	0	9	9.4	**22**	10		3	4				**7**				1.2	0.3			**1.5**	31	30-70
Seminars	5	4	1		0.2	0	0	**5.2**	5	0	1.5	4.6	0		0	**6.1**								**0**	11	10-30
Research	35	6	9	6	9.8	1	0.6	**32**	45	10	8.5	0	10	10	10	**49**	60	10	10	8.8	9.7	10	10	**59**	**139**	80-140
	60	10	10	10	10	10	10	**60**	60	0	13	8.6	10	10	10	**62**	60	10	10	10	10	10	10	**60**	**182**	180

3. Research activity
   Impedance spectroscopy (IS) is a powerful technique to quickly inspect material properties. This technique has been widely used in literature to characterize many devices, ranging from electrochemical to solid-state devices. This is an AC technique which allows the decoupling of the different contribution taking place at different frequency in the overall impedance. The advantage is that using this technique the contribution of specific interface can be investigated. In order to give a physical meaning to the extracted contribution, an equivalent circuit can be extracted from impedance data. This is not always a simple procedure due to the complexity of the structure under test. However, by extracting from the overall impedance the sole contribution of the junction capacitance it is possible to accurately characterize the junction. Capacitance versus voltage curve of a Schottky junction can give information on the barrier height or metal work function. These curves are usually analyzed inly in the forward bias in literature. Howbeit, the forward bias region is a valuable source of information. The interface can be characterized in terms of concentration of defects, if the C-V curve is considered in the forward bias region. This is the reason why an accurate study has to be done on such curves. The capacitance profile in forward bias condition exhibit a peak, differently from what the stated

by classical theory. Mathematical expression of this peak height and position in voltage have been found. It has also been investigated the link between such peak and some physical parameters, such as saturation current and series resistance. A TCAD model using Sentaurus Workbench environment has been built in order to study the influence of defects/traps on capacitance profile. Results demonstrate that fixed charges mostly affect the peak position while acceptors/donors traps modify the peak height. Moreover, it has been found in experimental data that sometimes there is an additional peak at high forward bias in capacitance. This second peak has been studied by means of TCAD model. The outcome revealed that this additional peak is an indicator of non-uniform properties of the interface. This can be used to understand if there are some problems in the device fabrication.

The C-V curves have been investigated also for SiC MOSFET structures. One of the still open issue for these devices is the higher traps density at the SiO_2/SiC interface. This is why one of the main challenges is the characterization of the interface traps. This is very complex and no accurate methods are available so far. This lack of information leads to the inaccurate modeling of the interface properties in TCAD simulations of SiC MOSFET devices. Even if TCAD simulators are a consolidated tool for the development of power semiconductor devices, an accurate model of the device is mandatory to carry out reliable simulations. For all these reasons, it has been exploited an accurate calibration of the TCAD model of a SiC MOSFET by means of different trap modelling of the SiO_2/SiC interface, depending on the SiC layer below the oxide. This result is very important because we have to think that technological steps of the two regions are different and hence the trap distribution is different. This proposed approach improves the predictability of the SiC MOSFET TCAD model, especially in reliability simulations, such as short-circuit or switching, where the temperature dependence of the threshold voltage, V_{TH}, is fundamental.

4. Products
    a. Publications

“Impedance Spectroscopy for the Characterization of the All-Carbon Graphene-Based Solar Cell” Matacena, I., Lancellotti, L., Lisi, N., Delli Veneri, P., Guerriero, P., & Daliento, S. Energies, 13(8), 1908. (2020).

“SiC MOSFET C-V Curves Analysis with Floating Drain Configuration” Ilaria Matacena, Luca Maresca, Michele Riccio, Andrea Irace, Giovanni Breglio and Santolo Daliento, Virtual Issue ECSCRM 2021.

“Experimental Analysis Of C-V and I-V Curves Hysteresis in SiC MOSFETs” Ilaria Matacena, Luca Maresca, Michele Riccio, Andrea Irace, Giovanni Breglio and Santolo Daliento. Virtual Issue ECSCRM 2021.

“TCAD model calibration for the SiC/SiO2 interface trap distribution of a planar SiC MOSFET” Luca Maresca, Ilaria Matacena, Michele Riccio, Andrea Irace, Giovanni Breglio and Santolo Daliento, WIPDA 2020

“Effectiveness of defects annealing in graphene-silicon schottky junction monitored by means of forward bias capacitance measurements” (Journal under submission)

5. Conferences and Seminars

This year I attended the following conference:

- WIPDA 2020 (oral online presentation)

6. Activity abroad
   This year I spent 3 months abroad as Visiting Researcher at Kyoto University of Advanced Science (KUAS).

7. Tutorship
   a. As Master of Science correlator, the Double Degree Lodz-Naples student Aleksandra Wierzynska has been supported by me for her MSc thesis.
   b. As Master of Science correlator, the student Claudia Arcone has been supported by me for her MSc thesis