
**PhD in Information Technology and Electrical Engineering**

**Università degli Studi di Napoli Federico II**

# PhD Student: Ilaria Matacena

**XXXIII Cycle**

**Training and Research Activities Report – Second Year**

**Tutor: Santolo Daliento**

1. Information
   I received the M. Sc. Degree in Electronic Engineering from University of Napoli 'Federico II' in December 2016. I belong to XXXIII cycle of Information Technology and Electrical Engineering (ITEE) PhD. My fellowship is financed by athenaeum. My tutor is Prof. Santolo Daliento.

2. Study and Training activities
   During this second year I followed courses provided from a PhD school to improve my knowledge in electronics for space applications. I attended some seminars to extend my culture in other topics of Information Technology.
   Study and training activities are summarized below:
   a. Seminars
      Matlab and embedded system" (0.4)

      "IEEEXploreTraining and Authorship Workshop" (0.5)

      "Robots in medical application an overview of the current medical robotics from the industry's point of view" (0.6)

      "Medical thermal therapy and monitoring using microwave". Lecturer: Mahta Moghaddah. Organizer: Prof. Iodice. (0.2)

      "Distributed radio systems,virtual ran and path to 5G", Lecturer: Luca D'antonio. Organizer: Prof. Capozzoli. (0.4)

      "How to turbo boost your PhD", Lecturer and Organizer: Antigone Marino. (4)

   b. External courses
      PhD school SIE (4)

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**Cycle XXXIII**

| | Credits year 1 | | | | | | | | Credits year 2 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Estimated | 1 bimonth | 2 bimonth | 3 bimonth | 4 bimonth | 5 bimonth | 6 bimonth | Summary | Estimated | 1 bimonth | 2 bimonth | 3 bimonth | 4 bimonth | 5 bimonth | 6 bimonth | Summary | Total | Check |
| **Modules** | 20 | 0 | 0 | 4 | 0 | 9 | 9.4 | 22 | 10 | | 3 | 4 | | | | 7 | 29 | 30-70 |
| **Seminars** | 5 | 4 | 1 | | 0.2 | 0 | 0 | 5.2 | 5 | 0 | 1.5 | 4.6 | 0 | | 0 | 6.1 | 11 | 10-30 |
| **Research** | 35 | 6 | 9 | 6 | 9.8 | 1 | 0.6 | 32 | 45 | 10 | 8.5 | 0 | 0 | 0 | 0 | 19 | 51 | 80-140 |
| | 60 | 10 | 10 | 10 | 10 | 10 | 10 | 60 | 60 | 0 | 13 | 8.6 | 0 | 0 | 0 | 32 | 92 | 180 |

3. Research activity
   Impedance spectroscopy (IS) is a powerful technique to quickly inspect material properties. This technique has been widely employed during years in various application fields, from

batteries to semiconductor devices. In particular, some features of p-n junctions can be drawn by analysing the junction capacitance at various DC biases. Indeed, Capacitance Voltage (C-V) measurements allow deep physical insight into recombination phenomena taking place at the junction. In the case of metal-semiconductor (MS) structures, the knowledge of the junction capacitance allows the extraction of the metal work function and the corresponding barrier height arising at the semiconductor side. A widely recognized issue is that capacitance contributions (different from the junction, such as the capacitance associated to contacts and semiconductor interfaces) can affect the measurements. In order to exactly extract the aforementioned physical parameters, it is necessary to isolate the junction capacitance from the total measured capacitance. On the other side, analysing capacitance contribution associated to contacts allows to investigate contact properties. Thus, the separation of capacitance contributions from the total capacitance value is of paramount importance. By analysing the overall impedance through IS, information can be achieved by means of equivalent circuit representation. Assuming that each interface can be associated to a resistance-capacitance (RC) parallel network, the total structure impedance can be modelled trough an equivalent circuit given by a series of RC pairs with a series resistance and eventually a series inductance. From the parameters of the equivalent circuit it is possible to extract relevant interface properties. The equivalent circuit extraction procedure is not universal neither automatic and it generally requires a good expertise. Pure mathematic fitting is not always a good strategy, resulting in parameters without any physical significance. Unfortunately, such a strategy is widely employed, due to large diffusion of commercial fitting software; despite that, interpretation of the results is often controversial, disregarding physical underlying mechanisms. Usually, the goodness of the equivalent circuit extraction procedure uniquely leans to the algorithm convergence, without considering physical constraints. This year research activity is related to an automatic procedure to accurately extract the equivalent circuit parameters from impedance spectroscopy data. The procedure automatically identifies a unique circuit schematic, suitable for all the considered DC bias voltages, while the corresponding resistance and capacitance values extracted are voltage dependent. The novelty of the proposed solution relies on the cross information gained by experimental Nyquist plots, to automatically assign initial values for the extraction procedure, and C-V plots, to ensure higher reliability than mere analytic fit.

Another concern in my research activity is the interface properties characterization of SiC MOSFETs. SiC MOSFETs are gradually replacing silicon power devices in many applications because of the higher performances of the material. Even if the technology for SiC MOSFET has been improved in the last years, the very high interface $SiO_2$/SiC trap density is still a problem that affects the present SiC MOSFET generations. This issue is still not addressed in TCAD simulations supporting the devices development. Traps distribution at such interface is complex and it affects the overall performance of the device. Traps influence both current-voltage and capacitance-voltage characteristics of a SiC MOSFET. The aim of my research is the study of interface traps effects on C-V and I-V curves for a 1200 V SiC MOSFET. The numerical study is adopted to explain the shape of experimental C-V curves of commercial devices. The effects on the C-V curve have been investigated, varying interface trap properties, such as traps type, energy level and density. A threshold voltage instability has been found, highlighting hysteresis effects both in current - voltage and capacitance - voltage curves. A hysteresis effect emerged from numerical transfer characteristics, when a trap distribution exists at SiC/SiO2 interface and this effect is more emphasized with decreasing temperature. Finally, experimental C-V curves of commercial SiC MOSFETs are compared to simulated results. These curves exhibit a very different trend from theoretical MOSFET C-V

curves. Similar non ideal behavior arises from numerical and experimental curves due to existing interface traps distribution.

4. Products
   a. Publications

I. Matacena, et al. “Impedance spectroscopy characterization of a graphene based solar cell with improved contacts”, ELECTRIMACS, 2019.

L. Lancellotti, N. Lisi, P. Delli Veneri, E. Bobeico, I. Matacena, P. Guerriero, S. Daliento “Graphene-on-Silicon solar cells with graphite contacts”, ICCEP, 2019.

P. Guerriero, C. Attanasio, I. Matacena, and S. Daliento “Merged photovoltaic/wave system for the power supply of a marine buoy for harbour monitoring”, ICCEP, 2019.
Matacena “Equivalent circuit extraction procedure from Nyquist plots for graphene-silicon solar cells”, PRIME, 2019.

L. Maresca, I. Matacena, M. Riccio, A. Irace, G. Breglio and S. Daliento “Influence of the SiC/SiO2 SiC MOSFET interface traps distribution on C-V measurements evaluated by TCAD simulations”. Journal of Emerging and Selected Topics in Power Electronics.

I. Matacena, L. Maresca, M. Riccio, A. Irace, G. Breglio and S. Daliento “Evaluation of interface traps type, energy level and density of SiC MOSFETs by means of C-V curves TCAD simulations” ICSCRM 2019

P. Guerriero, A.P. Catalano, I. Matacena, L. Codecasa, V. d’Alessandro, S. Daliento “Analysis of the yield reduction in PV plants due to partial shading and electrothermal effects”. THERMNIC 2019

I. Matacena “Impedance spectroscopy characterization of innovative graphene on silicon solar cells contacts”, SIE 2019

5. Conferences and Seminars

This year I attended the following conferences:

- ELECTRIMACS 2019, held in Salerno (oral presentation)
- SIE 2019, held in Rome (poster presentation)
- ICCEP 2019, held in Otranto (oral presentation)
- PRIME 2019, held in Lausanne (oral presentation)

6. Activity abroad

No activities abroad.

7. Tutorship

This year I finished the tutor scholarship. My work as tutor consisted of exercises on fundamental physics subjects (Fisica I).