PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Mirko Gagliardi

XXXI Cycle

Training and Research Activities Report – First Year

Tutor: Alessandro Cilardo

1. Information

- Mirko Gagliardi, master's degree in Computer Engineering in 2015 from the University of Naples Federico II.
- XXXI Cycle – ITEE
- Doctoral Fellowship funded by CeRICT
- Tutor: Alessandro Cilardo
- Collaboration with CeRICT in the context of European project MANGO. "MANGO: exploring Manycore Architectures for Next-GeneratiOn HPC systems" is a large-scale European project exploring heterogeneous manycore architectures for HPC, and innovative architectural mechanisms for High Performance, Power-efficiency and time-Predictability tomorrow HPC systems.

2. Study and Training activities

- MS Modules:
  i. *Advanced Computer Architecture and GPU Programming*, Alessandro Cilardo, 07/01/2016, 6 CFU;
  ii. *Intelligenza Artificiale*, Flora Amato, 26/09/2016, 6 CFU;
- Ad Hoc Modules:
  i. *Communicating and Disseminating your Research Work*, Mo Mansouri, 16/03/2016, 3 CFU;
  ii. *Scientific Writing*, Paolo Russo, 24/05/2016, 5 CFU;
- Seminars
  i. *Networks-On-Chip: Introduction And Advanced Topics*, Josè Flitch, 16/11/2015 – 18/11/2015, 1.8 CFU (1 extra credit for supplementary activities);
  ii. *Adversarial Testing of Protocol Implementations,* Prof. Cristina Nita Rotaru, 23/09/16, 0.4 CFU;
  iii. *Programmable Network conjugation*, Roberto Bifulco, 26/02/2016, 0.4 CFU;
  iv. *Speech Technologies At Trinity College*, Loredana Cerrato, 02/03/2016, 0.2 CFU;
  v. *Challenging Real-Time Measurement Systems For Immersive Life-Size Augmented Environment*, Giovanni Caturano, 29/04/2016, 0.5 CFU;
  vi. *Methodologies for embedded software validation*, Diego Tornese, 25/05/2016, 0.2 CFU;
  vii. *Internet: la dimensione immateriale dell'esistenza*, Stefano Quintarelli, 19/05/2016, 0.4 CFU;
  viii. *DDoS Detection in Cloud and Campus Networks*, Jill Jermin, 06/06/2016, 0.2 CFU;
  ix. *An Overview on Image Forensics with emphasis on physics-based scene verification*, Christian Riess, 18/05/2016, 0.2 CFU;
  x. *Half Day EMC Design and troubleshooting Course*, Arturo Mediano, 29/09/2016, 0.8 CFU;

	Credits year 1							
		1	2	3	4	5	6	
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary
Modules	20	0	6	3	5	0	6	**20**
Seminars	5	1,8	0,8	0,8	1,2	0	0,8	**5,4**
Research	35	7	4	6	5	8	5	**35**
	60	8,8	10,8	9,8	11,2	8,0	11,8	**60,4**

3. Research Activities

- Title: *Exploring Advanced Computer Architecture and Technique to Improve Performance and Power Efficiency in Many Core Era*

Nowadays, **Exascale Computing** is constantly gaining importance in the Scientific Community and **High-Performance Computers** are now considered essential for some experiments in many sectors, such as digital signal processing applications, scientific intense calculation, computer graphics and even cinematic applications. However, most high-performance architectures mostly rely on general-purpose compute units such as CPUs and/or GPUs, which deliver adequate performance while ensuring programmability and application portability. Unfortunately, pure general-purpose hardware is affected by inherently limited power-efficiency (low GFLOPS-per-Watt) now considered as a primary metric.

In this context, current trends in HPC are increasingly moving towards **heterogeneous platforms**, systems made of different computational units, with specialized accelerators that complement general purpose CPUs, including digital signal processors (DSPs) or graphics processing units (GPUs), co-processors, and custom acceleration logic, enabling significant benefits in terms of both power and performance. Historically, HPC has never extensively relied on **FPGAs**, mostly because of the reduced support for floating-point arithmetic, as FPGAs are typically fixed-point oriented. Modern **Altera** and **Xilinx** FPGA families focus on floating-point operations reaching **10 TFLOPs** ideal peak performance. Furthermore, FPGAs are historically power efficient. Those are the essential reasons while very recent trends

are putting more emphasis on the potential role of FPGAs, beyond very special-purpose acceleration. Architectural customization can play a key role in modern high-performance architectures, as it enables unprecedented levels of power-efficiency compared to CPUs/GPUs. In line with the above trends, academic and industrial research is focusing on **GPU-like** paradigms to introduce some form of programmability in FPGA design. In the last years, a few GPU-like projects have appeared, such as: Nyuzi, flexgrip, Maven VT, MIAOWGPU.

My research activity investigates the architectural requirements of emerging HPC applications and the most suitable power efficient and high performance solutions My final goal is to model application-driven accelerator based on GPU-like paradigm that can best fits new emerging HPC application requirements. In this context, our research group founded the **Nu+ project**.

Nu+ project main focus is parametrization. Our aim is to build an application-driven architecture to achieve the best hardware/software configuration for any data-parallel kernel. Specialized data-parallel accelerators have been known to provide efficiency than general-purpose processors for codes with significant amounts of regular data-level parallelism (DLP). However every parallel kernel has its own "ideal" configuration. The Nu+ architecture is a GPU-like open-source softcore. This HPC-oriented accelerator merges SIMT paradigm with a vector processor model. The core is RISC-based in-order pipeline. Its control unit is intentionally light. Our architecture masks memory and operation latencies deeply relaying on hardware multithreading. Our aim is to keep the architecture control logic light and focus on a heavily parallelism and high data-parallel kernel oriented.

Nu+ project is part of a larger H2020 project named MANGO. The main MANGO objective is to define new-generation high-performance, power-efficient, deeply heterogeneous architectures.

4. Products

- Publications:
    i. Cilardo Alessandro, Gagliardi Mirko. "*Customizable Heterogeneous Acceleration for Tomorrow's High-Performance Computing.*" High Performance Computing and Communications (HPCC), 2015 IEEE 7th International Symposium on Cyberspace Safety and Security (CSS), 2015 IEEE 12th International Conference on Embedded Software and Systems (ICESS), 2015 IEEE 17th International Conference on. IEEE, 2015.

ii. Cilardo Alessandro, Gagliardi Mirko, Donnarumma Ciro, "*A Configurable Shared Scratchpad Memory for GPU-like Processors*." International Conference on P2P, Parallel, Grid, Cloud and Internet Computing. Springer International Publishing, 2016.