PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Darjn Esposito

XXIX Cycle

Training and Research Activities Report – First Year

Tutor: Prof. Antonio Strollo

1. Information

I received the M. S. degree, cum laude, in Electronic Engineering from University of Napoli "Federico II". I belong to XXIX cycle of ITEE PhD. My fellowship is financed by DIETI for research in VLSI systems. My tutor is Prof. Antonio Strollo.

2. Study and Training activities

In this first year I followed courses to improve knowledge in VLSI systems and electronic devices (through PhD Schools), courses to improve research skills (through ad hoc modules of ITEE PhD), course to improve English language and to broaden my knowledge in topic near VLSI systems (through M. S. and B. S. DIETI courses and Occasionally provided courses of ITEE PhD).
To be more specific:

a. Courses
   - "Calcolatori Elettronici II", M. S. course, held by Prof. Nicola Mazzocca; 0 CFU
   - "Reti di Calcolatori", B. S. course, held by Prof. Antonio Pescapè, 0 CFU
   - "Corso di Europrogettazione", module for improvement of research skills, 3 CFU
   - "English Course - Preparation to Cambridge B1 Exam (PET)", held by CLA (Prof. Geraint Thomas), 3 CFU
   - "The Entrepreneurial Analysis of Engineering Research Projects", module for improvement of research skills, 3 CFU
   - "Three core issues for the Internet: things, security and economics", module "Occasionally provided", 2 CFU

b. Seminars
   - "Opportunities and Challenges in Two-Dimensional Magnetic Recording", Dr. Jonathan Coker, 2.4.2014, 0.2 CFU
   - "Circuiti Quantistici", Prof. Giovanni Miano, 4.4.2014, 0.2 CFU
   - "Novel Tendencies in Power Semiconductor Devices and Circuits", Prof. Alberto Castellazzi, 5-6 May 2014, 0.6 CFU
   - "Control System Design Using Energy Properties of Physical Systems", Dr. Alejandro Donaire, 23 June 2014, 0.2 CFU
   - "Smart Sensor and Actuators at the Age of Internet of Things", workshop, Organized by the LAB4MEMS ENIAC Project (EU), 29-30 August 2014, Bertinoro (Italy). (web: http://sinano2014.arces.unibo.it/), 1 CFU
   - "Fractional Programming for Energy Efficiency in Wireless Networks", Dr. Alessio Zappone, 15 and 22 September 2014, 0.6 CFU
   - "Towards agile flight of vision-controlled micro flying robots: from frame-based to event-based vision", Prof. Davide Scaramuzza, 16 September 2014, 0.2 CFU
   - Seminars-cycle, "Nano-Carbon Based Components and Materials for High-Frequency Electronics", Prof. Sergey Maksimenko, Prof. Gregory Slepyan, Prof. Pavel Dyachkov, Prof. Alexander Lobko, 6 October 2014, 0.8 CFU
   - "Quantum Teleportation", Prof. Giovanni Miano, 23 October 2014, 0.2 CFU
   - "Verification of Mobile Agents in Partially Known Environments", Dr. Sasha Rubin, 27 November 2014, 0.4 CFU
   - "Site Reliability Engineering at Google", Dr. Marco Papa Manzillo, 27 November 2014, 0.5 CFU
   - "Memory Technologies for Android Based Systems", Prof. Simon Pietro Romano, 5 December 2014, 0.4 CFU

c. External courses
   - "Essential verification with SystemVerilog and UVM", 2-6 June 2014, Imec, Kapeldreef 75, 3001 Leuven, Belgium. (web: http://www2.imec.be/be_en/home.html), 3 CFU
   - "GE Ph.D. School", 16-18 June 2014, University of Cagliari. (web: http://sites.unica.it/ge2014/scuola-di-dottorato/?lang=it), 3 CFU

- "Reliability and Variability of Electronic Devices", 6th European SINANO Summer School, 24-29 August 2014, Bertinoro (Italy). (web: http://sinano2014.arces.unibo.it/), 3 CFU

	Credits year 1							
		1	2	3	4	5	6	
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary
Modules	20	0	3	6	0	6	5	**20**
Seminars	5	0.4	0.8	1	1.8	1.3	0	**5.3**
Research	35	10	5	4	7	4	8	**38**
	60	10	8.8	11	8.8	11	13	**63**

Year	Lecture/Activity	Type	Credits	Certification	Notes
1	Calcolatori Elettronici II	MS Module	0		I only followed the course
1	Reti di Calcolatori	BS Module	0		I only followed the course
1	Corso di Europrogettazione	Ad hoc Module	3	x	
1	English Course - Preparation to Cambridge B1 Exam (PET)	External Course	3	x	Certification without CFU conversion. Followed at Centro Linguistico di Ateneo.
1	The Entrepreneurial Analysis of Engineering Research Projects	Ad hoc Module	3	x	
1	Three core issues for the Internet: things, security and economics	Ad hoc Module	2	x	
1	Essential verification with SystemVerilog and UVM	External Course	3	x	
1	Gruppo Elettronica Ph.D. School	Doctoral School	3	x	Certification without CFU conversion
1	Reliability and Variability of Electronic Devices	Doctoral School	3	x	
1	Opportunities and Challenges in Two-Dimensional Magnetic Reco	Seminar	0.2	x	
1	Circuiti Quantistici	Seminar	0.2	x	
1	Novel Tendencies in Power Semiconductor Devices and Circuits	Seminar	0.6	x	
1	Control System Design Using Energy Properties of Physical Syst	Seminar	0.2	x	
1	Smart Sensor and Actuators at the Age of Internet of Things	External Seminar	1	x	
1	Fractional Programming for Energy Efficiency in Wireless Networl	Seminar	0.6	x	
1	Towards agile flight of vision-controlled micro flying robots: from fr	Seminar	0.2	x	
1	Nano-Carbon Based Components and Materials for High-Frequen	Seminar	0.8	x	
1	Quantum Teleportation	Seminar	0.2	x	
1	Verification of Mobile Agents in Partially Known Environments	Seminar	0.4	x	
1	Site Reliability Engineering at Google	Seminar	0.5	x	
1	Memory Technologies for Android Based Systems	Seminar	0.4	x	

3. Research activity

My research activity is actually focused on "Speculative Parallel-Prefix adders". The speculation is a well-known technique used in computer architecture to "making the common case fast" [1], exploiting predictions. Recently, timing speculation have been proposed [2]-[8] at circuit level to improve functional units performance. In particular, my research activity focused on reducing adders' critical path, making carries predictions.

It is worthwhile observing that addition is a fundamental part of modern arithmetic operation: adders are wide used in microprocessors for address calculations as well as for floating point division and multiplication. Therefore, reducing adders' critical path can significantly improve pipelines' throughput. This represents one of the major challenges in digital designs. Let us recall that the bottleneck for speed in an adder is the carry computation. This prevents computing the sum bits in a perfect parallel way, since, in the worst case, a carry is generated in the *lsb* and propagates, through the whole adder, up to the *msb*.

A lot of adders have been proposed in literature, trading area for speed. Among these, the adders used in high-performance circuits (es. CPU, GPU) are parallel-prefix adders such as Brent-Kung [9], Kogge-Stone [10], Han-Carlson [11]. These topologies allows reaching the lower bound for delay, equal to $O(log_2(n))$ for a n-bit adder [12]. In order to overcome these bounds, speculation can be exploited, basing upon the observation that the critical path is rarely activated in traditional adders [2]-[6]. To this regard, [6] demonstrates that the carry propagation length doesn't exceed $K \approx O(log_2(n))$; therefore the events in which the carry propagates from *lsb* to *msb* (i.e. for n bits) are very rare. This allows simplifying carry computation, and turns into a faster adder, at the price of having, in rare cases (i.e. when the carry propagates for more than K bits), incorrect results. Therefore a speculative adder is augmented with an error detection network that asserts an output

signal when speculation fails. In this case (misprediction), another clock cycle is needed to obtain the correct result, with the help of a correction stage. Due to this feature, speculative adders are noted in literature as *variable latency speculative adders (VLSA).*

This study of literature has been fundamental in order to find some opportunities, in the current state of art, to improve VLSA performance. The key observation is that all the actual literature [6]-[8] is focused on developing VLSA based on the parallel-prefix Kogge-Stone adder. They implement a speculative Kogge-Stone, by pruning the last levels of the traditional Kogge-Stone topology. The main issue of a Kogge-Stone VLSA is that the error detection circuitry has a critical path delay comparable to that needed to compute the speculative sum. Therefore the advantage due to speculation can be degraded by the error detection.

Moved by this reason and by the lack in literature of VLSA based on others parallel-prefix topologies, I, with the collaboration of Professors A. Strollo, D. De Caro, N. Petra, E. Napoli, focused on developing an Han-Carlson VLSA. The choice of Han-Carlson topology is due to the fact that it can achieve equal speed performance respect to Kogge-Stone adder, at lower power consumption and area [13]. Therefore it is interesting to implement a speculative Han-Carlson adder. A relevant portion of the research activity has been devoted to understand how and which levels has to be pruned in order to develop a generalizable methodology to obtain a speculative Han-Carlson topology, chosen the *K* value.

After this step, great attention has been reserved to the implementation of error detection circuitry. Due to the last Brent-Kung carry merge level (absent in Kogge-Stone topology), the error detection circuitry is simpler and therefore faster, than that of Kogge-Stone speculative adder, previously developed in literature. During this step, a novel approach to error detection, in parallel-prefix adders, has been developed. Indeed, in the circuits proposed in literature, the error detection network checks a necessary only condition to have an error, therefore there are conditions in which the error detection circuitry detects some false positive errors, degrading the average addition time (defined in [14]). The proposed novel approach, obtained by developing a rigorous derivation of the error detection network, allows decreasing error probability (no false positive errors are detected), with benefits on the average addition time. Moreover, the proposed Han-Carlson VLSA topology, exhibits a lower error probability than Kogge-Stone VLSA.

After this theoretical analysis, supported by the developing of an analytical model to compare spatial complexity (i.e. an area estimation) and delay of the proposed VLSA with respect Kogge-Stone VLSA, Matlab scripts have been developed which generate Verilog descriptions of the proposed variable latency speculative adders, and of their non-speculative counterpart. After this phase, the proposed circuits have been simulated in order to verify the functionality. During this phase, Monte Carlo simulations have been performed, in order to obtain the error probability values, on varying of *K* parameter, for 32, 64 and 128 bits.

As final step, the adders have been synthesized in the UMC 65 nm library, on varying the synthesis timing constraint, in order to have a clear comparison of the best topology, as a function of the desired clock frequency. Both the Han-Carlson and Kogge-Stone VLSA, have been synthesized for different *K* values, in order to understand the optimal *K* value for each adder size *n.* The synthesis results show that proposed Han-Carlson VLSA outperforms previously developed variable latency Kogge-Stone architectures. Compared with traditional, non-speculative, adders, the results' analysis demonstrates that variable latency Han-Carlson adders show sensible improvements when the highest speed is required; otherwise the burden imposed by error detection and error correction stages overwhelms any advantage.

As next step, my research activity is actual focused to develop other parallel-prefix VLSA, such as Hybrid Han-Carlson [15], Brent-Kung [9], Carry-Increment [16]. A speculative Hybrid Han-Carlson topology has been actually developed and some preliminary results have been obtained, showing better results than Han-Carlson VLSA. Moreover, an effective implementation of VLSA working in applications where 2'complement representation is used, (i.e. long propagation chain due to sign extension) is one of the main goal of my next year research activity.

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[16] R. Zimmermann, "Binary Adder Architectures for Cell-Based VLSI and their Synthesis," Ph.D. thesis, Swiss Federal Institute of Technology, (ETH) Zurich, Hartung-Gorre Verlag, 1998.

4. Products

a. Journal papers

I. D. Esposito, D. De Caro, E. Napoli, N. Petra, A. G. M. Strollo, "Variable Latency Speculative Han-Carlson Adder", *Circuits and Systems I: Regular Papers, IEEE Transactions on,* accepted for publication, in press.

b. Conference papers

I. D. Esposito, D. De Caro, A. G. M. Strollo, "Speculative Parallel-Prefix Adders", *Proceedings of 46th GE Conference*, ISBN: 978-88-905519-2-5.
II. D. Esposito, D. De Caro, M. De Martino, A. G. M. Strollo, "Error Detection in Variable Latency Parallel-Prefix Speculative Adders", *13th IEEE International NEW Circuits And Systems (NEWCAS) conference,* submitted.
III. D. Esposito, D. De Caro, M. De Martino, A. G. M. Strollo, "Variable Latency Speculative Han–Carlson Adders Topologies", *11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015),* submitted.
IV. M. De Martino, D. Esposito, D. De Caro, N. Petra, A. G. M. Strollo, "Easy Clock Synchronization in Multi-domain Spread Spectrum Clocking Systems", *13th IEEE International NEW Circuits And Systems (NEWCAS) conference,* submitted.

5. Conferences and Seminars

Presentations made:
"Speculative Parallel-Prefix Adders", 46th GE Conference, Cagliari , June 18-20, 2014.

6. Activity abroad

I followed the course "Essential verification with SystemVerilog and UVM", 2-6 June 2014, at Imec research centre, Leuven, Belgium. (web: http://www2.imec.be/be_en/home.html).

7. Tutorship

a. Correlator for M. S. thesis, "Progetto di circuiti digitali dedicati al calcolo di funzioni non lineari", Student: Marco Prece , 20 hours.

b. Assistant for exercises of the M. S. course “Architettura dei sistemi integrati”, held by Prof. Antonio Strollo, 15 hours.