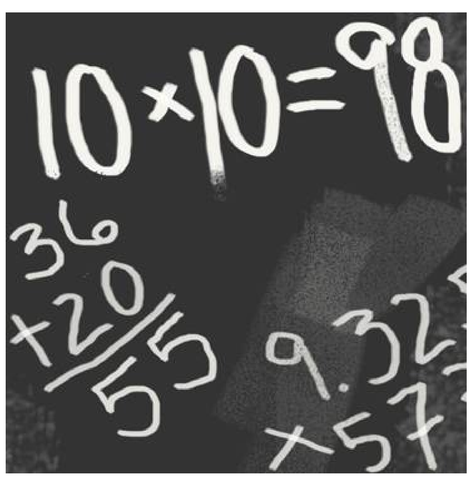
Darjn Esposito

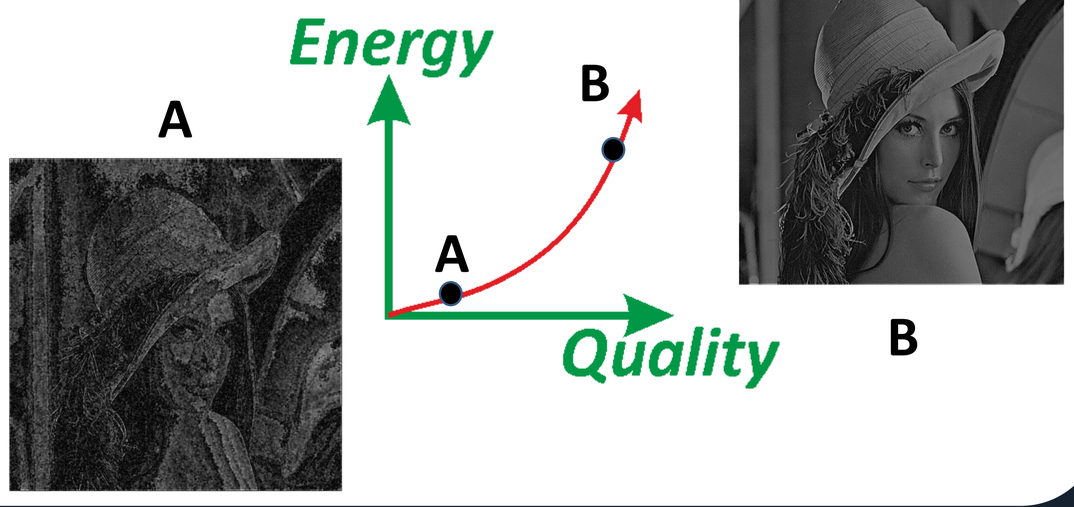
Tutor: Prof. Antonio Strollo

XXIX Cycle - II year presentation



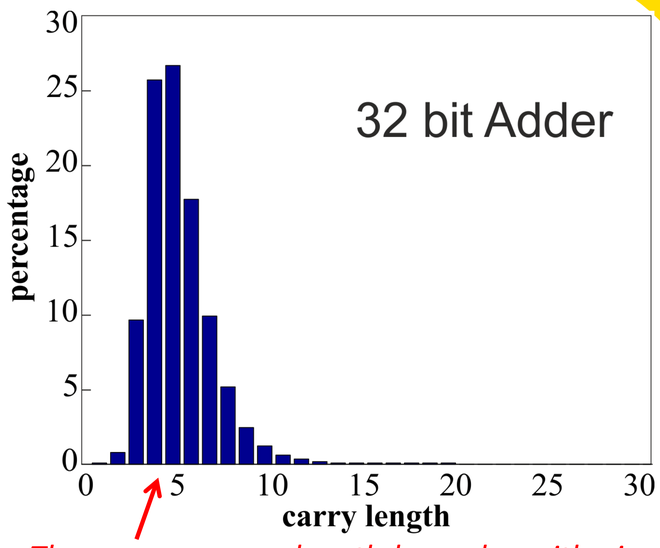
Approximate Computing

My research activity is focused on developing approximate and speculative arithmetic blocks. Indeed, by relaxing the requirement of performing exact calculations **more efficient** digital circuit can be designed.
Several applications show a good degree of resiliency to errors, such as multimedia processing, machine learning, data mining. For application that need perfect computations a speculative approach can be used (in case of error the result is corrected).

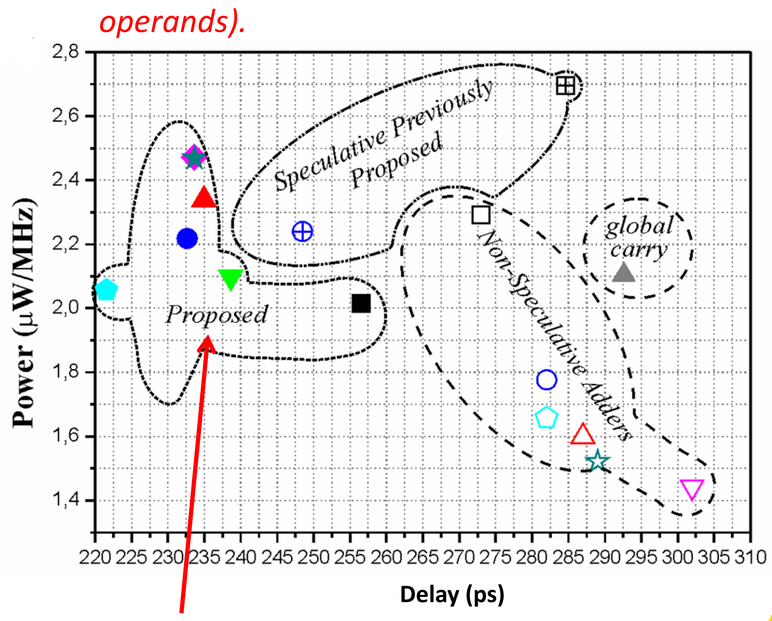


My research activity during this two years of PhD has involved adders:
Idea: Under independently and uniform input operands, the adder critical path is rarely activated. Employing this observation the circuitry of adders can be simplified by making speculations (predictions), at a price of having some rare incorrect results.
Developments: We applied this idea to develop novel speculative parallel-prefix adders [1], [2]. We developed also novel error detection and correction approaches (for application non error-resilient) to keep error rate low also with different input operands statistics (e.g. two'2 complement operands) [3].
We developed also approximate adders for error tolerant applications [4].
Results: The proposed adders outperform the previoulsy proposed speculative adders and the standard (non-speculative) adders when the highest speed is required.
Products:

[1] D. Esposito, D. De Caro, E. Napoli, N. Petra, A.G.M. Strollo, "Variable Latency Speculative Han-Carlson Adder," IEEE Trans. on Circuits and Systems I: Regular Papers, vol.62, no.5, pp.1353-1361, 2015.
[2] D. Esposito, D. De Caro, M. De Martino, A.G.M. Strollo, "Variable latency speculative Han-Carlson adders topologies," 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp.45-48, 2015.
[3] D. Esposito, D. De Caro, A.G.M. Strollo, "Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands," submitted to IEEE Trans. on Circuits and Systems I: Regular Papers.
[4] D. Esposito, G. Castellano, D. De Caro, E. Napoli, N. Petra, A.G.M. Strollo, "Approximate Adder With Output Correction for Error Tolerant Applications and Gaussian Distributed Inputs," accepted to IEEE International Symposium on circuits and systems (ISCAS) 2016.



The average carry length has a logarithmic behavior with adder size (hyp. Uniform operands).



Proposed speculative adders are faster than previously proposed in literature.

Cooperations: Green IC group, National University of Singapore.

NUS National University of Singapore

Green IC

Future Developments: I'm actually visiting student at National University of Singapore. I'm working on Multiply-and-Accumulate (MAC) units that can automatically tune the approximation level in function of the input data statistic.
The idea is to use these MAC units in Convolutional Neural Networks. The target is to design a chip which automatically tunes the energy-quality trade-off, in function of the input data statistics.