PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Darjn Esposito

XXIX Cycle

Training and Research Activities Report – Third Year

Tutor: Prof. Antonio Strollo

1. Information

I received the M. S. degree, cum laude, in Electronic Engineering from University of Napoli "Federico II". I belong to XXIX cycle of ITEE PhD. My fellowship is financed by DIETI for research in VLSI systems. My tutor is Prof. Antonio Strollo.

2. Study and Training activities

In this third year I followed courses and seminars to improve knowledge in VLSI systems and electronic devices.
To be more specific:

a. Seminars
- "Tamper Resistant Processors For The Internet Of Things", Prof. Patrich Schaumon, 8th March 2016, 0.2 CFU, followed at National University of Singapore.
- "What is an FPGA and When Would I use it?", Prof. Patrich Schaumon, 9th March 2016, 0.2 CFU, followed at National University of Singapore.
- "Clock Network Design for Ultra-Low Voltage Digital Integrated Circuits", Mr. Lin Longyang, 15th March 2016, followed at National University of Singapore.
- "Dynamically Reconfigurable Micro-Architecture For Wide Voltage Scaling", Mr. Saurabh Jain, 15th March 2016, 0.2 CFU, followed at National University of Singapore.
- "Prospects Of Efficient Neural Computing Using Cellular Array Of Magneto-Metallic Neurons And Synapses", Prof. Kaushik Roy, 17th March 2016, 0.2 CFU, followed at National University of Singapore.
- "A Case For Fine-Grain Processor Arrays For Efficient And High Performance Computation", Prof. Bevan Baas, 24th March 2016, 0.3 CFU, followed at National University of Singapore.
- "Device-Circuit Co-Design Of Multi-Gate FETs In Scaled Technologies", Prof. Kaushik Roy, 29th March 2016, 0.3 CFU, followed at National University of Singapore.
- "CMOS Ageing: Modelling, Monitoring and Mitigation", Prof. Mark Zwolinski, 27th April 2016, 0.2 CFU, followed at National University of Singapore.

b. External courses
- "Encounter Digital Implementation (Hierarchical)", held by Cadence Design Systems, Internet Learning Series, 18 September 2016, 1 CFU.

Student: Darjn Esposito									Tutor: Prof. Antonio Strollo								Cycle XXIX									
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	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0	3	6	0	6	5	20	10	0	9	0	0	1	0	10	0	0	0	0	1	0	0	1	31	30-70
Seminars	5	0.4	0.8	1	1.8	1.3	0	5.3	5	1.7	1.2	0	0.2	1.2	0	4.3	0	1.8	0	0	0	0	0	1.8	11.4	10-30
Research	35	10	5	4	7	4	8	38	45	8	10	8	8	8	6	48	60	10	10	10	10	6	6	52	138	80-140
	60	10.4	8.8	11	8.8	11.3	13	63.3	60	9.7	20.2	8	8.2	10.2	6	62.30	60	12	10	10	11	6	6	55	180.4	180

Year	Lecture/Activity	Type	Credits	Certification
1	Calcolatori Elettronici II	MS Module	0	
1	Reti di Calcolatori	BS Module	0	
1	Corso di Europrogettazione	Ad hoc Module	3	x
1	English Course - Preparation to Cambridge B1 Exam (PET)	External Course	3	x
1	The Entrepreneurial Analysis of Engineering Research Projects	Ad hoc Module	3	x
1	Three core issues for the Internet: things, security and economics	Ad hoc Module	2	x
1	Essential verification with SystemVerilog and UVM	External Course	3	x
1	Gruppo Elettronica Ph.D. School	Doctoral School	3	x
1	Reliability and Variability of Electronic Devices	Doctoral School	3	x
1	Opportunities and Challenges in Two-Dimensional Magnetic Recording	Seminar	0.2	x
1	Circuiti Quantistici	Seminar	0.2	x
1	Novel Tendencies in Power Semiconductor Devices and Circuits	Seminar	0.6	x
1	Control System Design Using Energy Properties of Physical Systems	Seminar	0.2	x
1	Smart Sensor and Actuators at the Age of Internet of Things	External Seminar	1	x
1	Fractional Programming for Energy Efficiency in Wireless Networks	Seminar	0.6	x
1	Towards agile flight of vision-controlled micro flying robots: from frame-based to event-based vision	Seminar	0.2	x
1	Nano-Carbon Based Components and Materials for High-Frequency Electronics	Seminar	0.8	x
1	Quantum Teleportation	Seminar	0.2	x
1	Verification of Mobile Agents in Partially Known Environments	Seminar	0.4	x
1	Site Reliability Engineering at Google	Seminar	0.5	x
1	Memory Technologies for Android Based Systems	Seminar	0.4	x
2	Affidabilità di Dispositivi e Moduli Elettronici	Seminar	1.2	x
2	The iCub project: An open platform for research in robotics & artificial intelligence	Seminar	0.3	x
2	Agents with truly Perfect Recall	Seminar	0.2	x
2	On Abel differential equations of the 2nd kind and exact inversion of boost DC/AC converters	Seminar	0.2	x
2	Lagrangean relaxation and Set Covering	Seminar	1	x
2	On the complexity of Temporal Equilibrium Logic	Seminar	0.2	x
2	English Course for PhD Students- B2 Level	External Course	6	x
2	Designing and writing scientific manuscripts for publication in english language scholarly journals, and related topics	Ad hoc Module	3	x
2	Test And Diagnosis of Integrated Circuits (17 Novembre, Alberto Bosio, Valentina Casola)	Seminar	1.2	x
2	Encounter Digital Implementation (Block)	External Course	1	x
3	Tamper Resistant Processors For The Internet Of Things	External Seminar	0.2	x
3	What is an FPGA and When Would I use it?	External Seminar	0.2	x
3	Clock Network Design for Ultra-Low Voltage Digital Integrated Circuits	External Seminar	0.2	x
3	Dynamically Reconfigurable Micro-Architecture For Wide Voltage Scaling	External Seminar	0.2	x
3	Prospects Of Efficient Neural Computing Using Cellular Array Of Magneto-Metallic Neurons And Synapses	External Seminar	0.2	x
3	A Case For Fine-Grain Processor Arrays For Efficient And High Performance Computation	External Seminar	0.3	x
3	Device-Circuit Co-Design Of Multi-Gate FETs In Scaled Technologies	External Seminar	0.3	x
3	CMOS Ageing: Modelling, Monitoring and Mitigation	External Seminar	0.2	x
3	Encounter Digital Implementation (Hierarchical)	External Course	1	x

3. Research activity

In the third year of PhD I focused on speculative adders for MAC units and on precision-scalable units. These activities are classifiable in the big framework of “Approximate Computing” [1]-[6]. By relaxing the requisite of exact computations, substantial improvement can be obtained in digital circuits [7], [8]. Several applications, spanning from multimedia to machine learning [4], [9] exhibit an excellent grade of resiliency, therefore they output are lightly compromised by errors during the processing.

Recently, precision-scalable systems have been proposed, based on the observation that the degree of resilience varies greatly, depending on the input data being processed [10]-[12]. In this context I worked on precision-scalable Multiply-and-Accumulate units and memories.

Multipliers constitute one of the most energy-hungry fundamental digital block [13], therefore many researches focused on energy-efficient implementation. I focused on programmable truncated multiplier [14]. Briefly, in some digital signal processing applications it is possible discarding the least significant columns in the partial product matrix [15]-[17]. This gives advantages in terms of dynamic power dissipation, since the least significant columns are usually freezed to zero, reducing the switching activity of the multiplier. The idea of discard some columns in the partial product matrix is possible since the LSB of the multiplication result has a precision that is higher of that of input

operands. Usually, a compensation mechanism is employed to compensate the discarded columns [17]. My contribution focused on implementing a real-time data-aware compensation technique which negligible energy overhead. This results in the first hardware implementation of compensation technique for precision-scalable truncated multiplier. The committed errors, due to precision scalability, are subsampled and their mean error is evaluated. A control circuit allows to compensate the committed mean error when this is non-zero. An aggressive subsample rate is employed, therefore the overhead resulting by the compensation circuit is negligible in terms of power dissipation. Since the compensation mechanism evaluates the real committed errors in order to choose and update the compensation term, a data-aware compensation mechanism is obtained. The compensation term, therefore, exhibits an adaptive behaviour in function of the the input data. The comparison with the other compensation techniques shows that proposed approach is able to adapt to different dataset providing significantly improved quality results where the other technique fails and equal quality results where other compensation technique alternate their domain. In terms of quality-power tradeoff, proposed MAC Unit with Real-Time Data-Aware compensation technique exhibits improved quality-energy performance for deeply-scaled precision level, allowing to shift the energy bound toward higher energy efficiency levels. The proposed MAC has been employed on some Convolutional Neural Network kernels showing an always better energy-quality tradeoff than precision-scalable MAC with no compensation technique.

Moreover an approximate precision-scalable MAC unit has been investigated. In a first approximation step, operated at design time, the MAC partial product terms are compressed by using simple OR gates as approximate counters [18], [19]. A second approximation step, tunable at run-time, allows to further save energy by turning-off selected columns of the partial product terms. A compensation term is introduced in the proposed MAC, to reduce the overall approximation error. A MAC unit, specialized to perform 2D convolution, is designed following the proposed approach and implemented in TSMC 40nm technology. The proposed circuit achieves power savings up to 53%, compared to standard, exact MAC, with tolerable image quality degradation.

While the majority of approximate computing papers focus on approximate arithmetic units (see, e.g., [20]-[21]), some papers investigate methods to perform energy-quality scaling in SRAM and DRAM memories [22]-[23], while Standard Cell Memories have not been investigated to the best of our knowledge. Standard Cell Memories (SCMs) represent an interesting alternative to conventional SRAM arrays when implementing embedded memories [24]. SCMs store information in arrays of flip-flops or latches. They can be described using HDL languages and easily synthesized in an automated manner, being composed of standard cells. This allows high design flexibility at very low design effort, since the memory features (e.g., number of ports, words and wordlength) are defined through simple HDL coding and without the limitations imposed by the usage of memory generators [25]. Also, SCMs are well known to be able to operate at much lower voltages (i.e., energy) than conventional SRAMs [24]-[25]. SCMs also improve area efficiency, for memory banks with kbit-range capacity [24], [26]. In addition, SCMs can be placed and routed automatically, and hence merged with logic blocks, improving data locality with consequent reduction of wiring and parasitics (i.e. improved energy efficiency and timing). As an example, this property was leveraged in [27] to devise a placement methodology to optimize density and power, as part of an automated digital design flow.

In particular, I proposed a precision-scalable latch-based memory for the first time, allowing to adjust the trade-off between dynamic power dissipation and quality. The proposed latch memory can be used as embedded array in precision-scalable systems. The fundamental idea is to group the *C* latches belonging to every row in one or more precision-scalable groups (*PSG*), which can be activated or deactivated as function of the desired quality or the input data statistics. The number and the group size of the PSG can be decided at design time, based on the targeted precision range of the system in which the memory are embedded, and the word size. Post-layout simulations show that power dissipation is reduced more than 60% compared to conventional SCMs. This comes at negligible image quality degradation (SSIM=0.99) at reasonably large resolutions (e.g., 16 bits), at which the power consumption is higher and hence the proposed technique is highly relevant. Developed precision-scalable MAC units and precision-scalable SCM can be employed in a precision-scalable datapath, as an example for computer vision applications.

Finally, the use of approximate adders as final adder of carry-save multiplier-accumulators (MACs) has been investigated for image processing applications. Many papers have introduced approximate adders for image processing application, but their investigations are done making assumptions that

are hardly verified in practical applications. As an example, [28] employs approximate adders for image processing applications, but the multiplications and subtraction are performed by exact functional units. Similar assumption are done in [29]. The use of approximate adders and the consequent performance improvement strictly depends on the input statistics of the approximate adder [21], [30], therefore on the application. We propose a design flow to opportunely design the approximate adders accounting for the input distribution.

The MAC employed in this paper is constituted by a carry-save Wallace tree for partial product compression. The resulting output, in carry-save format, is added using an approximated carry-propagate adder. We start the MAC design describing its architecture in HDL language. The HDL code is then read and optimized by the synthesizer. In this phase the synthesizers detects the arithmetic operator and performs datapath extraction to opportunely transform the arithmetic operators into optimized blocks. In this phase carry-save arithmetic is usually employed in order to optimize datapath performance. A final carry-propagate adder is then employed to sum the output of the carry-save stage, obtaining the final result.

Unfortunately, describing the MAC operation as y<=A+B*C, the designer is not able to access, after the synthesis, to the carry-save signals to be summed by the final adder. To overcome this issue, we employ arithmetic IP components to describe the MAC. In particular, in Cadence RTL Compiler synthesizer the designer can use the ChipWare IP Components [31], in Synopsys Design Compiler the designer can use DesignWare Building Block IP [32]. Therefore a design flow has been proposed to accurately choose the approximate adder architecture as a function of the application. The image filtering results have shown that, for some kernel filters the approximation results in significant noise, affecting the overall image quality. To mitigate this phenomena, a simple technique has been employed which allows skipping the erroneous pixel, using the previous, corrected one. This improves quality sensibly. The VLSI implementation results show that use of speculative adders as final adder in MAC units allows saving 15% of power in voltage scaled mode. Moreover, it has been observed that this gain can increase if the speculative adder is designed accounting for the non-uniform arrival time of the carry-save signals.

Note that part of the third year activities have been developed during the visiting at National University of Singapore.

[1] K. Roy, A. Raghunathan, “Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications”, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, 2015, pp. 473-475.

[2] S. Venkataramani, S. T. Chakradhar, K. Roy, A. Raghunathan, "Approximate computing and the quest for computing efficiency," *Design Automation Conference (DAC), 2015 52nd ACM/EDAC/IEEE*, San Francisco, CA, 2015, pp. 1-6.

[3] S. Venkataramani, S. T. Chakradhar, K. Roy, A. Raghunathan, "Computing approximately, and efficiently," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2015, Grenoble, 2015, pp. 748-751.

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[5] S. Mittal, “A Survey of Techniques for Approximate Computing”, *ACM Computing Surveys,* 2016.

[6] J. Han, M. Orshansky, "Approximate computing: an emerging paradigm for energy-efficient design", proc. 18th IEEE Europ. Test Symp., pp. 1-6, May 2013.

[7] S.-L. Lu, "Speeding up processing with approximation circuits," *Computer* , vol.37, no.3, pp.67,73, Mar 2004.

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[10] V. Chippa, A. Raghunathan, K. Roy and S. Chakradhar, "Dynamic effort scaling: Managing the quality-efficiency tradeoff," Design Automation Conference (DAC), 2011 48th ACM/EDAC/IEEE, New York, NY, 2011, pp. 603-608.

[11] B. Moons and M. Verhelst, "A 0.3–2.6 TOPS/W precision-scalable processor for real-time large-scale ConvNets," 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, 2016, pp. 1-2.

[12] A. Raha, H. Jayakumar and V. Raghunathan, "Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 3, pp. 846-857, March 2016.

[13] M. Horowitz, "1.1 Computing's energy problem (and what we can do about it)," 2014 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2014, pp. 10-14.

[14] M. de la Guia Solaz, W. Han and R. Conway, "A Flexible Low Power DSP With a Programmable Truncated Multiplier," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 11, pp. 2555-2568, Nov. 2012.

[15] M. Schulte and E. E. Swartzlander Jr., "Truncated multiplication with correction constant [for DSP]", Proc.Workshop VLSI Signal Process. VI, pp. 388-396, 1993

[16] A. Strollo , N. Petra and D. DeCaro, "Dual-tree error compensation for high performance fixed-width multipliers", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 8, pp. 501-507, 2005.

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[19] I. Qiqieh, R. Shafik, G. Tarawneh, D. Sokolov, A. Yakovlev, "Energy-Efficient Approximate Multiplier using Bit Significance-Driven Logic Compression", accepted at Design, Automation and Test in Europe 2017 (DATE) conference.
[20] H. Jiang, J. Han, F. Lombardi, "A comparative review and evaluation of approximate adders", Proc. of Great Lakes Symposium on VLSI, pp. 343-348, Pittsburgh, 2015.
[21] D. Esposito, G. Castellano, D. De Caro, E. Napoli, N. Petra and A. G. M. Strollo, "Approximate adder with output correction for error tolerant applications and Gaussian distributed inputs," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 1970-1973.
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[28] C. Liu, J. Han, F. Lombardi, "An analytical framework for evaluating the error characteristics of approximate adders", IEEE Trans. on Computer, vol. 64, n. 5, pp.1268-1281, May 2015.
[29] A. B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," DAC Design Automation Conference 2012, San Francisco, CA, 2012, pp. 820-825.
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[31] ChipWare IP Components in Encounter® RTL Compiler, Cadence, Product Version 14.2, August 2015.
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4. Products (accounting also the first and second PhD years)

a. Journal papers

I. **D. Esposito**, D. De Caro, E. Napoli, N. Petra, A. G. M. Strollo, "Variable Latency Speculative Han-Carlson Adder", ***IEEE Trans. on Circuits and Systems I: Regular Papers***, vol.62, no.5, pp.1353-1361, 2015.

II. **D. Esposito**, D. De Caro and A. G. M. Strollo, *"Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands," in* ***IEEE Transactions on Circuits and Systems I: Regular Papers***, vol. 63, no. 8, pp. 1200-1209, Aug. 2016.

III. E. Napoli, G. Castellano, D. De Caro, **D. Esposito**, N. Petra and A. G. M. Strollo, *"A SISO Register Circuit Tailored for Input Data with Low Transition Probability," in* ***IEEE Transactions on Computers***, vol. 66, no. 1, pp. 45-51, Jan. 1 2017.

IV. E. Napoli; G. Castellano; D. De Caro; **D. Esposito**; N. Petra; A. G. M. Strollo, *"Single Bit Filtering Circuit Implemented in a System for the Generation of Colored Noise," in* ***IEEE Transactions on Circuits and Systems I: Regular Papers*** , vol.PP, no.99, pp.1-11.

V. D. De Caro; E. Napoli; **D. Esposito**; G. Castellano; N. Petra; A. G. M. Strollo, *"Minimizing Coefficients Wordlength for Piecewise-Polynomial Hardware Function Evaluation With Exact or Faithful Rounding," in* ***IEEE Transactions on Circuits and Systems I: Regular Papers*** , vol.PP, no.99, pp.1-14.

VI. G. Castellano, D. De Caro, **D. Esposito**, P. Bifulco, E. Napoli, N. Petra, M. Romano, M. Cesarelli, A.G.M. Strollo, " A Hardware Oriented Real Time Filter for Poisson Video Denoising with Application to X-ray Fluoroscopy", **submitted** to ***IEEE Trans. on IEEE Transactions on Circuits and Systems for Video Technology***

b. Conference papers

I. **D. Esposito**, D. De Caro, A. G. M. Strollo, "Speculative Parallel-Prefix Adders", *Proceedings of 46th GE Conference*, ISBN: 978-88-905519-2-5.

II. **D. Esposito**, D. De Caro, M. De Martino, A. G. M. Strollo, "Variable Latency Speculative Han–Carlson Adders Topologies", ***11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015)***, pp.45-48, 2015.
III. **D. Esposito**, G. Castellano, D. De Caro, E. Napoli, N. Petra and A. G. M. Strollo, "Approximate adder with output correction for error tolerant applications and Gaussian distributed inputs," 2016 ***IEEE International Symposium on Circuits and Systems (ISCAS)***, Montreal, QC, 2016, pp. 1970-1973.
IV. E. Napoli, G. Castellano, **D. Esposito** and A. G. M. Strollo, "Digital circuit for the generation of colored noise exploiting single bit pseudo random sequence," *2016* ***IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS)***, Florianopolis, 2016, pp. 23-26.
V. **D. Esposito**, A. G. M. Strollo, M. Alioto, "Power-Precision Scalable Latch Memories", accepted at ***2017 IEEE International Symposium on Circuits and Systems (ISCAS)***, Baltimore, MD, USA.
VI. **D. Esposito**, D. De Caro, E. Napoli, N. Petra, A. G. M. Strollo, "On the Use of Approximate Adders in Carry-Save Multiplier-Accumulators", accepted at ***2017 IEEE International Symposium on Circuits and Systems (ISCAS)***, Baltimore, MD, USA.
VII. **D. Esposito**, A. G. M. Strollo, M. Alioto, "Low-Power Approximate MAC Unit", submitted at ***13th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2017)***.

5. Conferences and Seminars

Presentations made:

I. *"Speculative Parallel-Prefix Adders", 46th GE Conference,* Cagliari , June 18-20, 2014. (first PhD year)
II. *"Variable Latency Speculative Han–Carlson Adders Topologies",* ***11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015),*** Glasgow, July 2015. (Second PhD year). **Bronze Leaf Award**.

6. Activity abroad

I. I followed the course "Essential verification with SystemVerilog and UVM", 2-6 June 2014, at **Imec research centre**, Leuven, Belgium. (web: http://www2.imec.be/be_en/home.html).
II. Visiting PhD student at **National University of Singapore, Green IC Group** (3rd January 2017-3rd July 2017) (second-third year). During this activity one publication has been produced, one has been submitted and we are attending the response (while a chip in CMOS 28nm is in design phase):
    a. **D. Esposito**, A. G. M. Strollo, M. Alioto, "Power-Precision Scalable Latch Memories", **accepted** at ***2017 IEEE International Symposium on Circuits and Systems (ISCAS)***, Baltimore, MD, USA.
    b. **D. Esposito**, A. G. M. Strollo, M. Alioto, "Low-Power Approximate MAC Unit", **submitted** at ***13th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2017)***.

7. Tutorship

a. Correlator for M. S. thesis, "Progetto di circuiti digitali dedicati al calcolo di funzioni non lineari", Student: Marco Prece , 20 hours. (first PhD year)
b. Assistant for exercises of the M. S. course "Architettura dei sistemi integrati", held by Prof. Antonio Strollo, 15 hours. (first PhD year)

c. Correlator for M. S. thesis, “Progetto ed implementazione su FPGA di un filtro spazio-temporale per applicazioni fluoroscopiche basato su approccio IIR”, Student: Antonino Battaglia , 10 hours. (second PhD year)
d. Assistant for exercises of the B. S. course “Sistemi Elettronici Programmabili”, held by Prof. Ettore Napoli, 15 hours. (second PhD year)
e. Assistant for exercises of the M. S. course “Architettura dei sistemi integrati”, held by Prof. Antonio Strollo, 10 hours. (second PhD year)
f. Assistant for exercises of the M. S. course “Architettura dei sistemi integrati”, held by Prof. Antonio Strollo, 15 hours. (third PhD year)