PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Darjn Esposito

XXIX Cycle

Training and Research Activities Report – Second Year

Tutor: Prof. Antonio Strollo

1. Information

I received the M. S. degree, cum laude, in Electronic Engineering from University of Napoli "Federico II". I belong to XXIX cycle of ITEE PhD. My fellowship is financed by DIETI for research in VLSI systems. My tutor is Prof. Antonio Strollo.

2. Study and Training activities

In this second year I followed courses to improve knowledge in VLSI systems and electronic devices, courses to improve research skills (through ad hoc modules of ITEE PhD) and course to improve English language.
To be more specific:

a. Courses
- "Designing and writing scientific manuscripts for publication in english language scholarly journals, and related topics", Ad hoc Module, held by Prof. Barnett Parker, 3 CFU
- "English Course for PhD Students- B2 Level", held by CLA (Prof. Dianna Pickens), 6 CFU

b. Seminars
- "Affidabilità di Dispositivi e Moduli Elettronici", Prof. Alberto Castellazzi, 24-25-26 March 2015, 1.2 CFU
- "The iCub project: An open platform for research in robotics & artificial intelligence", Dr. Giorgio Metta, 18.3.2015, 0.3 CFU
- "Agents with truly Perfect Recall", Dr. Nills Bulling, 28 April 2015, 0.2 CFU
- "On Abel differential equations of the 2nd kind and exact inversion of boost DC/AC converters", Dr. Joseph M. Olm, 13 May 2015, 0.2 CFU
- "Lagrangean relaxation and Set Covering", Prof. Manlio Gaudioso, 3 June 2015,1 CFU
- "On the complexity of Temporal Equilibrium Logic", Dr. Laura Bozzelli, 22 October 2015, 0.2 CFU
- "Test And Diagnosis of Integrated Circuits (17 Novembre, Alberto Bosio, Valentina Casola)", Dr. Alberto Bosio, 17 November 2015, 1.2 CFU

c. External courses
- "Encounter Digital Implementation (Block)", held by Cadence Design Systems, Internet Learning Series, 16 November 2015, 1 CFU

	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0	3	6	0	6	5	20	10	0	9	0	0	1	0	10	0							0	30	30-70
Seminars	5	0,4	0,8	1	1,8	1,3	0	5,3	5	1,7	1,2	0	0,2	1,2	0	4,3	1							0	9,6	10-30
Research	35	10	5	4	7	4	8	38	45	8	10	8	8	8	6	48	59							0	86	80-140
	60	10,4	8,8	11	8,8	11,3	13	63	60	9,7	20,2	8	8,2	10,2	6	62,30	60	0	0	0	0	0	0	0	126	180

Year	Lecture/Activity	Type	Credits	Certification	Notes
2	Affidabilità di Dispositivi e Moduli Elettronici	Seminar	1,2	x	
2	The iCub project: An open platform for research in robotics & artificial intelligence	Seminar	0,3	x	
2	Agents with truly Perfect Recall	Seminar	0,2	x	
2	On Abel differential equations of the 2nd kind and exact inversion of boost DC/AC converters	Seminar	0,2	x	
2	Lagrangean relaxation and Set Covering	Seminar	1	x	
2	On the complexity of Temporal Equilibrium Logic	Seminar	0,2	x	
2	English Course for PhD Students- B2 Level	External Course	6	x	Certification without CFU conversion. Followed at Centro Linguistico di Ateneo.
2	Designing and writing scientific manuscripts for publication in english language scholarly journals, and related topics	Ad hoc Module	3	x	Certification must be provided by Prof. Riccio
2	Test And Diagnosis of Integrated Circuits (17 Novembre, Alberto Bosio, Valentina Casola)	Seminar	1,2	x	
2	Encounter Digital Implementation (Block)	External Course	1	x	Certification without CFU conversion

3. Research activity

In the second year of this PhD, I expanded the research work of the first year, meanwhile, during the last months of the second year I've started to enlarge my research interest to applications resilient to computational errors, in the framework of "Approximate Computing" [1]-[5].
In the first year my research was focused on "Speculative Parallel-Prefix adders". Briefly, by making "prediction" or "speculation" about the generation and the average carry length, adders architecture can be simplified (with benefits in terms of speed/area/energy), at the price of having some, rare, incorrect results [6]-[12]. During this first year my interest was therefore focused on "Speculative Computing", which can be considered as a subset of "Approximate Computing". In particular, a speculative adder can be augmented with error detection and correction circuitries, in this way, when a misprediction occurs, the result is corrected in an additional clock cycle, constituting a Variable-Latency-Speculative-Adder (VLSA) [10]-[12].
While in the first year my research was focused on developing an Han-Carlson VLSA [13], in the second year I, with the collaboration of Professors A. Strollo and D. De Caro, expanded the speculative approach to other parallel prefix topologies. In particular, we developed VLSAs for the following topologies: Brent-Kung [14], Hybrid Han-Carlson [15], Ladner-Fisher [16], Sklansky [17], Carry increment [18].
Moreover, as reported in [11], [12], when the input operands are no longer uniformly distributed (this occurs in applications using two's complement representation), the average carry length increases considerably, becoming comparable to the adder size. In this cases a large rate of mispredictions occurs, invalidating the effectiveness of speculative approach. Both [10]-[11] consider an additional carry signal, named "global carry" to reduce the rate of misprediction. triggered in presence of a long carry chain. This global carry is taken into account in the approximate adder by using additional logic levels that negatively affects overall performance of the speculative adder. Therefore we focused on developing effective error detection and correction approaches for VLSA working with two's complement operands, obtaining better performance than previously proposed approaches.
During second year, part of the research was devoted to approximate adders for error tolerant applications [8], [19]-[21]. In particular, we developed an approximate adder with a correction circuit that drastically reduces the error rate for Gaussian distributed operands (two's complement operands can be modelled as Gaussian distributed [11], [12]).
In the last months of the second year, I focused on programmable truncated multiplier [22]. Briefly, in some digital signal processing applications it is possible discarding the least significant columns in the partial product matrix [23]-[25]. This gives advantages in terms of dynamic power dissipation, since the least significant columns are usually freezed to zero, reducing the switching activity of the multiplier. The idea of discard some columns in the partial product matrix is possible since the LSB of the multiplication result has a precision that is higher of that of input operands. Usually, a compensation mechanism is employed to compensate the discarded columns. In [22] the activation-deactivation of the columns is controlled at run-time through a software approach. My research, starting from [22], is actually devoted to implement an hardware approach to estimate the error committed (due to the deactivation of columns) and to control this error by changing, at run-time, the number of activated columns. The run-time control is fundamental to guarantee the desired quality of the result on varying the data input statistics. This multiplier will be used in a MAC (multiply and accumulate unit) for error tolerant applications, such as image processing, machine learning

(convolutional neural network), in order to effectively employ the energy-quality trade-off that exists in these applications. I'm actually working on this idea as visiting PhD student at National University of Singapore.

[1] K. Roy, A. Raghunathan, "Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications", *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, 2015, pp. 473-475.
[2] S. Venkataramani, S. T. Chakradhar, K. Roy, A. Raghunathan, "Approximate computing and the quest for computing efficiency," *Design Automation Conference (DAC), 2015 52nd ACM/EDAC/IEEE*, San Francisco, CA, 2015, pp. 1-6.
[3] S. Venkataramani, S. T. Chakradhar, K. Roy, A. Raghunathan, "Computing approximately, and efficiently," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2015, Grenoble, 2015, pp. 748-751.
[4] Q. Xu, N. S. Kim, T. Mytkowicz, "Approximate Computing: A Survey," in *IEEE Design & Test*, vol. 33, no. 1, pp. 8-22, Feb. 2016.
[5] S. Mittal, "A Survey of Techniques for Approximate Computing", *ACM Computing Surveys,* 2016.
[6] S.-L. Lu, "Speeding up processing with approximation circuits," *Computer* , vol.37, no.3, pp.67,73, Mar 2004.
[7] T. Liu; S.-L. Lu, "Performance improvement with circuit-level speculation," *Microarchitecture,2000. MICRO-33. Proceedings. 33rd Annual IEEE/ACM International Symposium on* , vol., no., pp.348,355, 2000.
[8] N. Zhu; W.-L. Goh; K.-S. Yeo, "An enhanced low-power high-speed Adder For Error-Tolerant application," *Integrated Circuits, ISIC '09. Proceedings of the 2009 12th International Symposium on* , vol., no., pp.69,72, 14-16 Dec. 2009.
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[16] R.E. Ladner, M.J. Fischer, "Parallel Prefix Computation," Journal of the ACM, Vol. 27, No 4, October 1980, pp 831-838.
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[25] N. Petra , D. De Caro , V. Garofalo , E. Napoli and A. Strollo, "Truncated binary multipliers with variable correction and minimum mean square error", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1312-1325, 2010.

4. Products (for the first and second PhD years)

a. Journal papers

I. D. Esposito, D. De Caro, E. Napoli, N. Petra, A. G. M. Strollo, "Variable Latency Speculative Han-Carlson Adder", *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol.62, no.5, pp.1353-1361, 2015.

II. D. Esposito, D. De Caro, A. G. M. Strollo, "Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands," submitted to *IEEE Trans. on Circuits and Systems I: Regular Papers*.

III. E. Napoli, G. Castellano, D. De Caro, D. Esposito, N. Petra, A.G.M. Strollo, "A SISO register circuit tailored for input data with low transition probability," submitted to *IEEE Trans. On Computers.*

IV. G. Castellano, D. De Caro, D. Esposito, P. Bifulco, E. Napoli, N. Petra, M. Romano, M. Cesarelli, A.G.M. Strollo, "A Real-Time Spatio-Temporal IIR Filter for Poisson

Video Denoising with Application to X-ray Fluoroscopy", submitted to *IEEE Trans. on IEEE Transactions on Circuits and Systems for Video Technology*

b. Conference papers

I. D. Esposito, D. De Caro, A. G. M. Strollo, “Speculative Parallel-Prefix Adders", *Proceedings of 46th GE Conference*, ISBN: 978-88-905519-2-5.
II. D. Esposito, D. De Caro, M. De Martino, A. G. M. Strollo, “Variable Latency Speculative Han–Carlson Adders Topologies”, *11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015)*, pp.45-48, 2015.
III. D. Esposito, G. Castellano, D. De Caro, E. Napoli, N. Petra, A.G.M. Strollo, "Approximate Adder With Output Correction for Error Tolerant Applications and Gaussian Distributed Inputs," accepted to *IEEE International Symposium on circuits and systems (ISCAS) 2016*.
IV. E. Napoli, G. Castellano, D. Esposito, A. G. M. Strollo, “Digital Circuit for the Generation of Colored Noise Exploiting Single Bit Pseudo Random Sequence,” accepted to *IEEE LASCAS 2016.*

5. Conferences and Seminars

Presentations made:

I. *“Speculative Parallel-Prefix Adders”, 46th GE Conference,* Cagliari , June 18-20, 2014. (first PhD year)
II. *“Variable Latency Speculative Han–Carlson Adders Topologies”, 11th Conference on PhD Research in Microelectronics and Electronics,* Glasgow, July 2015. (Second PhD year). Bronze Leaf Award.

6. Activity abroad

I. I followed the course “Essential verification with SystemVerilog and UVM”, 2-6 June 2014, at Imec research centre, Leuven, Belgium. (web: http://www2.imec.be/be_en/home.html).
II. I’m actually visiting PhD student at National University of Singapore, Green IC Group.

7. Tutorship

a. Correlator for M. S. thesis, “Progetto di circuiti digitali dedicati al calcolo di funzioni non lineari”, Student: Marco Prece , 20 hours. (first PhD year)
b. Assistant for exercises of the M. S. course “Architettura dei sistemi integrati”, held by Prof. Antonio Strollo, 15 hours. (first PhD year)
c. Correlator for M. S. thesis, “Progetto ed implementazione su FPGA di un filtro spazio-temporale per applicazioni fluoroscopiche basato su approccio IIR”, Student: Antonino Battaglia , 10 hours. (second PhD year)
d. Assistant for exercises of the B. S. course “Sistemi Elettronici Programmabili”, held by Prof. Ettore Napoli, 15 hours. (second PhD year)
e. Assistant for exercises of the M. S. course “Architettura dei sistemi integrati”, held by Prof. Antonio Strollo, 10 hours. (second PhD year)