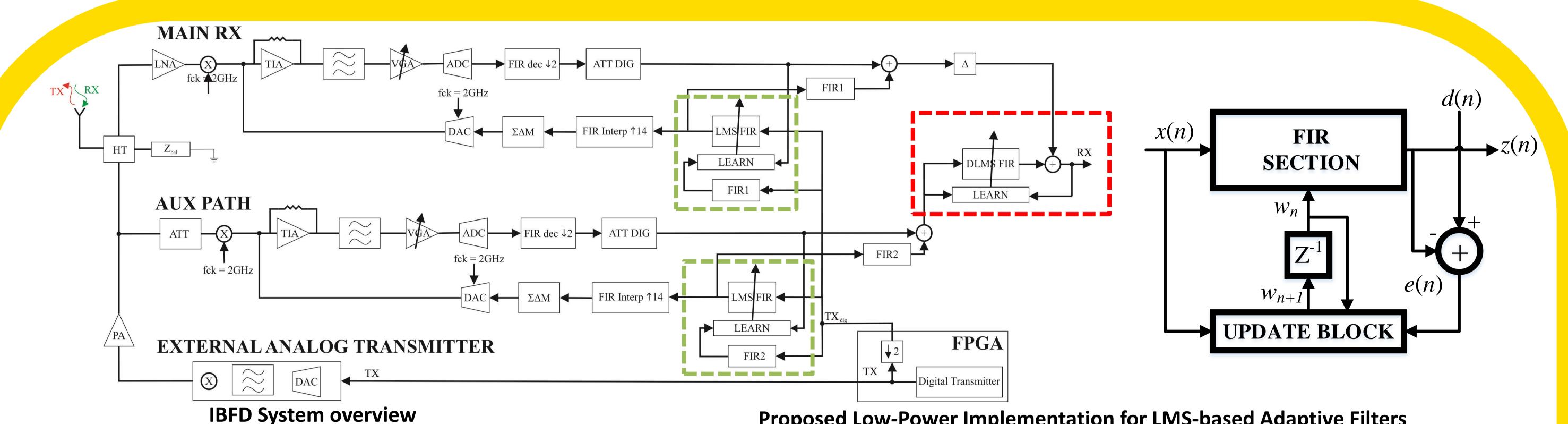
Gennaro Di Meo Tutor: Prof. Davide De Caro XXXIV Cycle - II year presentation

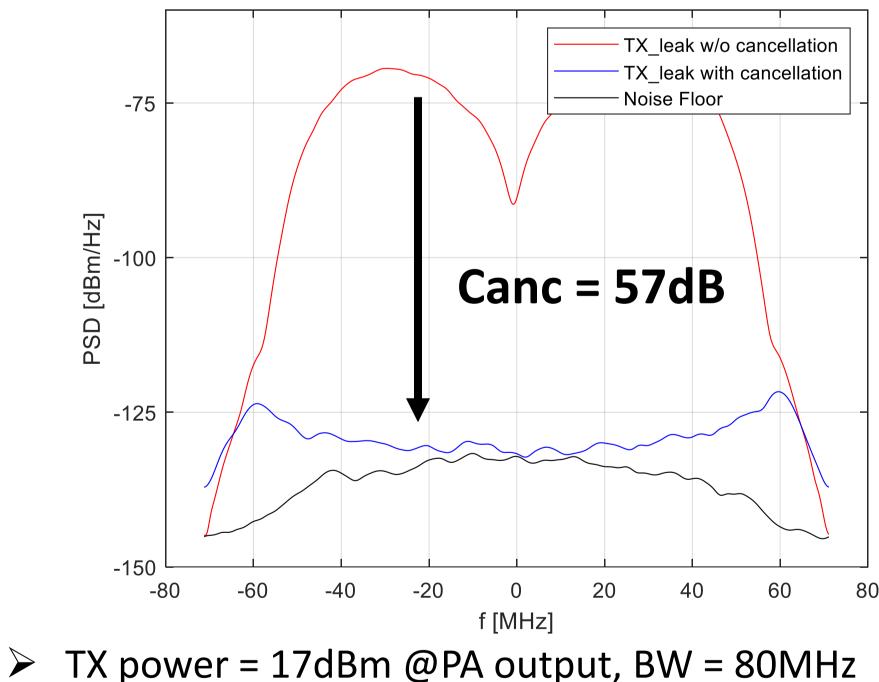
Digital Cancellation Techniques Toward Full-Duplex Radios

This research activity focused on the study of Digital Cancellation Techniques with application in the In-Band Full-Duplex (IBFD) communication. The IBFD paradigm provides to receive and to transmit signals sharing the same antenna and the same bandwidth at the same time, thus providing the possibility to double the channel capability. In an IBFD transceiver, strong coupling effects between the TX and the RX signals increase the receiver noise floor, thus cancellation techniques are required in order to improve the receiver sensitivity. In this contest, Adaptive Filters (AFs) are studied in order to suppress the TX leakage. In particular, this research activity addressed the implementation of AFs based on the Least Mean Square (LMS) algorithm and the development of optimized implementations in order to achieve high isolation levels with low-power features.



Proposed Low-Power Implementation for LMS-based Adaptive Filters

- Double path receiver architecture to delete nonlinearities of the power amplifier (PA)
- Hybrid Transformer (HT) for a first analog isolation
- DLMS filter (red box) to complete the TX leakage suppression
- Filtered-x LMS filters (green boxes) to reduce the power of signals in the Main RX and in the Aux Path
- Digital interpolation before the DACs to reduce phase noise disturbances



 \succ TX leakage power = 10dBm @Main RX output Noise Floor = -51 dBm @Main RX output

LMS algorithm updates filter taps according to the following equations:

- $\succ z(n) = \mathbf{w}_n \cdot \mathbf{x}(n)$ for output computation
- $\succ \mathbf{w}_{n+1} = \mathbf{w}_n + \mu e(n) \mathbf{x}(n)$ for coefficient learning

Power improvement is achieved by means of:

- \succ variable rounding on $\mathbf{x}(n)$ defined at runtime according to e(n) magnitude in the feedback
- switching activity reduction of multipliers in the update block of the AF

In addition, the approximation error is moderated by e(n) at regime.

Hardware performances are obtained by placing and routing the LMS filter in TSMC 28nm CMOS technology with core power supply of 0.9V and $f_{clock} = 200$ MHz.

In the proposed implementation, 2 and 4 LSBs of x(n) are rounded to zero when e(n) is low with power saving up to 27% and a negligible degradation of regime MSE.

		Regime MSE (system identification)			Dynamic Power [µW/MHz]			Area [mm ²]
		LP FIR	LP IIR	HP IIR	LP FIR	LP IIR	HP IIR	
Standard LMS		-64.54dB	-55.13dB	-45.39dB	245	251	259	0.081
Esposito et al., ISCAS 2018		-53.12dB	-49.57dB	-44.79dB	190 (-22.5%)	191 (-23.9%)	195 (-24.7%)	0.070 (-13.6%)
Esposito et al., ICECS 2018	THR=16	-47.66dB	-43.34dB	-41.39dB	198 (-19.2%)	209 (-16.7%)	219 (-15.4%)	0.087 (+7.4%)
Jiang et al., TCAS-I 2019		-46.38dB	-45.72dB	-42.41dB	143 (-41.6%)	160 (-36.3%)	168 (-35.1%)	0.052 (-35.8%)
Proposed technique		-64.51dB	-55.12dB	-45.38dB	181 (-26%)	184 (-27%)	204 (-22%)	0.082 (+1.2%)

The aforementioned technique is improved for the AFs employed in the IBFD system. Here, the absolute value |e(n)| is used to feed multipliers in the feedback. In this way, multipliers switching activity is further reduced since MSBs of |e(n)| are frozen to zero at regime. In addition, in the case of the DLMS filter, also fixed-width multipliers are employed to improve hardware performances of the FIR section of the AF. Results reveal a power consumption saving up to 58.9% at the cost of an acceptable increase of the area (+19%).

- \blacktriangleright Required cancellation = 61dB
- Actual effective cancellation = 57dB
- Simulink and Matlab to simulate the whole system
- System Verilog description of analog part to allow simulation by using the HDL language

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