PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Di Meo Gennaro

XXXIV Cycle

Training and Research Activities Report – Third Year

Tutor: Davide De Caro

Add the following items according to our meeting we have.

Concerning the structure of the document, use the Section number as is. Use the sub-contents indicated with a letter only as a suggestion for your content (a free form text is preferable)

1. Information
    a. Name Surname, MS title – University
    b. XXIX Cycle- ITEE – Università di Napoli Federico II
    c. Fellowship type
    d. Tutor
2. Study and Training activities
    a. Courses
    b. Seminars
    c. External courses
3. Research activity
    a. Title
    b. Study
    c. Research description
    d. Collaborations
4. Products
    a. Publications
        i. Books, Book Chapters, Journal papers, Conference papers (mark international products)
        ii. List those in preparation
    b. Patents
5. Conferences and Seminars
    a. Details (Conference name, place, dates, number of papers)
    b. Presentations made
6. Activity abroad
    a. Details (Place, dates, number of papers, contact persons)
7. Tutorship
    a. Type, subjects, hours

Information

Gennaro Di Meo graduated in Electronic Engineering at the University of Naples "Federico II" presenting "Design and Simulation of Adaptive Filters for Full-Duplex Radios in FinFET 14 nm CMOS Technology". Actually, he is a PhD Student (ministerial scholarship) at the Dept. of Electrical Engineering and Information Technology of the University of Naples Federico II (XXXIV Cycle - ITEE). The research activity of the PhD is focused on adaptive filters implementation (with special emphasis on application to in-band full-duplex RF communications) and adaptive low-power techniques for digital arithmetic circuits, under the supervision of Professor Davide De Caro.

Study and Training activities

Courses:

- Advanced synthesis with Genus Synthesis Solution v16.2 (Online), by Cadence
- Innovus Implementation System (Block) v20.1 (Online), by Cadence
- Innovus Implementation System (Hierarchical) v20.1 (Online), by Cadence
- Innovus Clock Concurrent optimization technology for clock tree synthesis v20.1 (Online), by Cadence

Seminars:

- Seminars from "Picariello Lectures on Data Science":
  - Digital project management: practices, processes, techniques, tools and scientific approach
  - #andràtuttobene: Images, texts, emojis and geodata in a sentiment analysis pipeline
  - At the nexus of big data, machine intelligence, and human cognition
  - Exploiting deep learning and probabilistic modeling for behavioral analytics
  - Data driven transformation in WINDTRE through managers voice
  - From photometric redshifts to improved weather forecasts an interdisciplinary view on machine learning
  - Cybercrime and e-evidence: the international legal framework for an effective criminal justice response
  - Artificial intelligence for natory's sector – a case study
  - The era of Industry 4.0: new frontiers in business model innovation
  - Approaches to graph machine learning
- Patent searching best practice
- Force and visual control of save human – robot interaction

- Beyond Einstein gravity: dark energy and dark matter as curvature effects
- The Ohta-Kawasaki model for diblok copolymers: stability and minimality of critical points
- Network Systems, Kuramoto Oscillators, and synchronous power flow
- Quasars as high redshift standard candles
- Advanced in machine learning for modelling and understanding the Earth sciences
- Dai mainframe all'IoT: una retrospettica sull'evoluzione delle architetture di calcolo
- Emotions in reinforcement learning agents
- Optimize graph representations for Right-Wing Reddit Community using graph neural network
- Short and ultrashort, high voltage electric pulses for biological and medical applications
- L'avvincente storia degli acceleatori
- Strategie terapeutiche innovative in campo immunologico: l'elettroporazione per la veicolazione di molecole farmacologiche
- 5G: l'architettura, le applicazioni e la rete di accesso

Student: Gennaro Di Meo									Tutor: Davide De Caro									Cycle XXXIV									
gennaro.dimeo@unina.it									davide.decaro@unina.it																		
	Credits year 1								Credits year 2									Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6				1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0,4	5	0	10	6	0	21	10	0	6,3	2	4	0	0	12		0	0	0	0	0	0	0	33,7	30-70
Seminars	5	0	0	1,5	1,4	0	0,4	3,3	5	0,8	0	1,1	2,3	0	1,2	5,4		1,7	0,3	0,8	1,3	2,3	0	6,4	15,1	10-30
Research	35	9,6	5	8,5	0	4	9,6	37	45	9,2	3,7	7	3,7	10	8,8	42		8,3	9,7	9,2	8,7	7,7	10	54	132,7	80-140
	60	10	10	10	11	10	10	61	60	10	10	10	10	10	10	60	0	10	10	10	10	10	10	60	181,5	180

Figure 1 – Credits Summary, third year.

Research activity

Digital cancellation techniques toward Full-Duplex radios

This research activity is focused on the study of digital cancellation techniques with application for the In-Band Full-Duplex (IBFD) communication. IBFD communication is a challenging technique that provides to simultaneously transmit and to receive signals by using the same bandwidth and the same antenna, offering the possibility to double the channel capacity. To that purpose, in a full-duplex transceiver the transmission (TX) and the reception (RX) paths should be isolated in order to avoid the superimposition of TX signal on the RX one. Devices as hybrid transformers could be employed for the achievement of a first isolation in the analog domain. Since the

cancellation capabilities depend on the antenna impedance variations and the signal bandwidth, further cancellation techniques are required in order to achieve the desired performances. In this contest, the Adaptive Filters (AFs) are studied with the aim to delete the interference in the digital domain. The AFs are able to change their impulse response minimizing the Mean Square Error (MSE) between their output and an external solicitation, allowing operations as system identification, channel equalization, and noise cancellation (of interest in this case). Among different topologies, Least Mean Square (LMS) filters are surely the most used thanks to their simple hardware structure, but also other variants are proposed in Literature according to different requirements. In the case of the analyzed system, Delayed LMS (DLMS) filters and filtered-x LMS filters are employed to achieve the required isolation.

This research activity is conducted in collaboration with University of Pavia and University of Milano "Bicocca" with the challenging aim to provide an experimental verification of studied techniques through the realization of a test-chip in advanced CMOS technology implementing a complete receiver with in-band full-duplex capability.

The first part of the third year was focused on the submission of the chip with the first In-Band Full-Duplex receiver. In particular, the following points were addressed:

- Design of a fast Successive Approximation Algorithm (SAR) for a 10-bits ADC, able to work at the challenging frequency of 3.4GHz
- Optimization of the digital logic aimed to program the 2GHz DACs involved in the self-interference cancellation
- Design of a Data-Weighted Averaging (DWA) algorithm for the reduction of the effects of the DAC current mismatches on the cancellation
- Improvement of the design of the filtered-x LMS algorithm and of the programmable finite impulse response filters used for the interference cancellation
- Design of a Built-In Self-Test (BIST) logic for the verification of the AFs
- Design of a Direct Digital Frequency Synthesizer (DDS) for the testing of the DACs and the ADCs used in the chip

After the chip submission, the research activity focused on the experimental verification of a chip fabricated in March 2019. This chip implements a novel approximate low-power DLMS with regime performances comparable to the exact version of the filter. The measurements, focused on the analysis of the power consumption, reveal the possibility to achieve up to 45.4% of power saving with respect to the exact implementation at the cost of an acceptable increase of the area occupation (+21.7%). This study was published in a journal paper (see the next section).

In addition, the digital parts of two mixed-signal systems were designed for the production of two chips in collaboration with the University of Pavia and the University of Milano "Bicocca", respectively. In the first chip, the digital circuits manage a 2-GHz DAC designed for the suppression of the self-interference in full-duplex transceivers. In the second chip, a SAR logic was designed in the contest of the PRIN project 2017. These chips, realized in TSMC 28nm CMOS technology, were submitted in May 2021 and August 2021.

Finally, the study of the digitally controlled delay lines (DCDLs) have been addressed in the second part of the year. This research deals with the analysis of the NAND-based, double-output DCDLs and of the glitch occurrences. A novel low-power, low-area, driving circuit, able to impose the delay in the DCDL, is proposed. In addition, along with the NAND-based topology, a novel inverter based DCDL has been proposed with the aim to further reduce the complexity of the driving circuit. This activity is in progress.

Products

Publications:

1. G. D. Meo, D. De Caro, G. Saggese, E. Napoli, N. Petra and A. G. M. Strollo, "A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, doi: 10.1109/TCSI.2021.3088913.

Conferences

1. Presentation of paper "Low-power Implementation of LMS Adaptive Filters Using Scalable Rounding", at IEEE International Symposium on Integrated Circuits and Systems 2020, virtual conference, 23-25 November 2020.

Tutorship

1. Co-supervisor of MSc student (Francesco Vistocco), analysis peak detection algorithm for Electro Cardio Gram (ECG) with implementations on DSP processors