PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Gennaro Di Meo

XXXIV Cycle

Training and Research Activities Report – Second Year

Tutor: Davide De Caro

Add the following items according to the meeting we had today.

Concerning the structure of the document, use the Section number as is. Use the sub-contents indicated with a letter only as a suggestion for your content (a free form text is preferable)

1. Information
    a. Name Surname, MS title – University
    b. XXIX Cycle- ITEE – Università di Napoli Federico II
    c. Fellowship type
    d. Tutor
2. Study and Training activities
    a. Courses
    b. Seminars
    c. External courses
3. Research activity
    a. Title
    b. Study
    c. Research description
    d. Collaborations
4. Products
    a. Publications
        i. Books, Book Chapters, Journal papers, Conference papers (mark international products)
        ii. List those in preparation
    b. Patents
5. Conferences and Seminars
    a. Details (Conference name, place, dates, number of papers)
    b. Presentations made
6. Activity abroad
    a. Details (Place, dates, number of papers, contact persons)
7. Tutorship
    a. Type, subjects, hours

Information

Gennaro Di Meo graduated in Electronic Engineering at the University of Naples "Federico II" presenting "Design and Simulation of Adaptive Filters for Full-Duplex Radios in FinFET 14 nm CMOS Technology". Actually, he is a PhD Student (ministerial scholarship) at the Dept. of Electrical Engineering and Information Technology of the University of Naples Federico II (XXXIV Cycle - ITEE). The research activity of the PhD is focused on adaptive filters implementation (with special emphasis on application to in-band full-duplex RF communications) and adaptive low-power techniques for digital arithmetic circuits, under the supervision of Professor Davide De Caro.

Study and Training activities

Courses:

1. Safety critical systems for railway traffic management
2. Scientific programming and visualization with Python
3. Matlab Fundamentals
4. Virtualization technologies and their applications

Seminars:

1. Lo spazio cibernetico come dominio bellico
2. Deep Learning Onramp
3. Computational Biology
4. Elettromagnetismo e Salute
5. Step into the world of packaging design rules, by Europractice
6. How to get published with the IEEE
7. Access the eLearning Library
8. Large Scale Training of Deep Neural Networks
9. SAS Analytics
10. Virtual Seminar on Sensing
11. Noninvasive Mapping of Electrical Properties using MRI
12. How to publish Open Access with IEEE to Increase the Exposure and Impact of your Research
13. Valutazione dei livelli di esposizione e del rispetto dei limiti Antenne e 5G
14. Misure di segnali complessi nell'ambiente: Sistemi 5G
15. Estrapolazioni su segnali 4G e 5G

Student: Gennaro Di Meo									Tutor: Davide De Caro								Cycle XXXIV									
gen.dimeo@unina.it									davide.decaro@unina.it																	
	Credits year 1								Credits year 2								Credits year 3									
	Estimated	1 bimonth	2 bimonth	3 bimonth	4 bimonth	5 bimonth	6 bimonth	Summary	Estimated	1 bimonth	2 bimonth	3 bimonth	4 bimonth	5 bimonth	6 bimonth	Summary	Estimated	1 bimonth	2 bimonth	3 bimonth	4 bimonth	5 bimonth	6 bimonth	Summary	Total	Check
Modules	20	0,4	5	0	10	6	0	21	10	0	6,3	2	4	0	0	12								0	34	30-70
Seminars	5	0	0	1,5	1,4	0	0,4	3,3	5	0,8	0	1,1	2,3	0	1,2	5,4								0	8,7	10-30
Research	35	9,6	5	8,5	0	4	9,6	37	45	9,2	3,7	7	3,7	10	8,8	42								0	79	80-140
	60	10	10	10	11	10	10	61	60	10	10	10	10	10	10	60	0	0	0	0	0	0	0	0	122	180

Fig. 1 - Credits Summary, year 2

Research activity

Digital cancellation techniques toward Full-Duplex radios

This research activity is focused on the study of digital cancellation techniques with application for the In-Band Full-Duplex (IBFD) communication. IBFD communication is a challenging technique that provides to transmit and to receive signals by using the same bandwidth at the same time, offering the possibility to double the channel capacity. To that purpose, in a full-duplex transceiver transmission (TX) and reception (RX) paths, connected to the same antenna, should be isolated in order to avoid the superimposition of TX signal on the RX one. Devices as hybrid transformers could be employed to achieve the required isolation in the analog domain, but, since interference cancellation is dependent on impedance balancing and frequency response shape, digital cancellation techniques are required in order to achieve the desired performances and extend the cancellation bandwidth. In particular, Adaptive Filters are studied. These circuits are able to change their impulse response minimizing the Mean Square Error (MSE) between their output and an external solicitation, allowing operations as system identification, channel equalization or noise cancellation (of interest in this case). Among different topologies, Least Mean Square (LMS) filters are surely the most used thanks to their simple hardware structure, but also other variants are proposed in Literature according to different requirements. In the case of the analyzed system, Delay-LMS filters and filtered-x LMS filters are employed to achieve the required isolation.

This research activity is conducted in collaboration with University of Pavia and University of Milano Bicocca with the challenging aim to provide an experimental verification of studied techniques through the realization of a test-chip in advanced CMOS technology implementing a complete transceiver with in-band full-duplex capability.

In this context, while the first year was spent to develop a reliable model of the proposed Full-Duplex system, in the second year the circuit that implements the digital part of the first IBFD chip was developed. The activity provided the following steps:

1) Verilog description of Delay-LMS and filtered-x LMS filters for the realization of the circuit
2) Development and improvement of low-power techniques aimed to reduce power consumption in adaptive filters with a negligible worsening of performances
3) Study of approximate multipliers (fixed-width topology and with approximate 4-2 compressors) for low-power purposes
4) Description and implementation of SAR logic for the ADCs required to implement the transceiver prototype (ADCs developed in collaboration with University of Milano Bicocca)
5) Description and implementation of digital up sampling logic (2GHz FIR interpolators), Sigma-Delta Modulators and digital logic for the DACs required by the transceiver prototype (DACs developed in collaboration with University of Pavia)

Actually, the digital part of the system provides the usage of two filtered-x LMS adaptive filters (that relax the linearity requirements of analog circuits) and a Delay-LMS filter (used to suppress the TX leakage).

At the same time, an intensive simulation activity was conducted in order to improve the description of the model used to analyze the cancellation. In particular, the analog part of the system (previously described by means of Matlab scripts and Simulink) was translated in System Verilog with the aim to improve integration and simulation capability with the HDL language.

Results, obtained by means of post place and route simulations in TSMC 28nm CMOS technology and clock frequency of 150MHz, reveal the possibility to implement a 22-taps complex high-cancellation Delay-LMS filter with a power consumption of 42.2mW, whereas the filtered-x LMS filter exhibits a power dissipation of 52.1mW with 20 complex taps. It is worth noting that the higher power consumption of the filtered-x LMS filter is due to the presence of two additive programmable FIR filters aimed to realize the adaptive algorithm and to improve the cancellation capability of the Delay-LMS filter. Low-power performances are achieved by leveraging the LMS error features at regime, by dynamically changing the precision of input signal in the feedback path of the filter, and by using approximate multipliers in the FIR section. The overall achieved power dissipation reduction is about 59% with respect to a standard implementation. At the same time, system simulations showed the possibility to reduce the TX leakage to the power level of the receiver noise floor by means of a digital cancellation of about 57dB.

The submission of the test-chip to the silicon foundry for its realization and the subsequent chip testing and measurements are scheduled for the third year of activity.

Products

Publications:

1. A.G.M. Strollo, E. Napoli, D. De Caro, N. Petra, G. Di Meo, “Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.67, no.9, pp. 3021-3034, Sept. 2020.
2. D. De Caro, G. Di Meo, E. Napoli, N. Petra and A.G.M. Strollo, "A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3839-3852, Nov. 2020.
3. G. Di Meo, D. De Caro, E. Napoli, N. Petra, A.G.M. Strollo, “Variable-Rounded LMS Filter for Low-Power Applications,” *Lecture Notes in Electrical Engineering*, vol.627, pp.155-161, 2020.
4. G. Di Meo, D. De Caro, E. Napoli, N. Petra, A.G.M Strollo, “Low-power implementation of LMS Adaptive Filter Using Scalable Rounding”, *2020 IEEE International Conference on Electronic Circuits and Systems* (accepted)
5. A.G.M. Strollo, D. De Caro, E. Napoli, N. Petra and G. Di Meo, "Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sevilla, 2020, pp. 1-4

Conferences

1. Presentation of paper “A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications”,
   at IEEE International Symposium on Integrated Circuits and Systems 2020, virtual conference, 27-28 August 2020.
2. Presentation of paper “Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor”,
   at IEEE International Symposium on Circuits and Systems, virtual conference, 10-21 October 2020.

Other Activities

One week at the University of Milano “Bicocca” to test the ditigal/analog interface of a chip produced in March 2019 in the context of PRIN project.

Tutorship

1. Co-supervisor of MSc student (Salvatore Montella), analysis of Digital Controlled Delay Lines