Antonio Pio Catalano

Tutor: Prof. Vincenzo d'Alessandro

XXXII Cycle - III year presentation

Numerical simulations and analytical modeling of the thermal and electrothermal behavior of electronic components and packages

Background

Master of Science	Ph.D.
Electronics Engineering – October 27th 2016 Subject : **Microelectronics**, Prof. *Vincenzo d'Alessandro*	Electronics Group – **Ing-Inf/01** Prof. **Vincenzo d'Alessandro** **Athenaeum** fellowship

Credit summary

Student: Antonio Pio Catalano								Tutor: Prof. Vincenzo d'Alessandro								Cycle XXXII									
antoniopio.catalano@unina.it								vindales@unina.it																	
Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	3	0	0	0	3	9	**15**	10	0	0	4	0	0	5	**9**	0	0	0	0	0	0	9	**9**	**33**	30-70
Seminars	5	1.9	0	0	3	0.8	0.3	**6**	5	0	0.4	0.5	0	0	0	**0.9**	0	0	0.8	0.5	0	2.1	0	**3.4**	**10**	10-30
Research	35	5.1	10	10	5	5.2	3.7	**39**	45	10	9.6	7.5	8	10	5	**50**	60	8	9.2	11	8	7.9	4	**48**	**137**	80-140
	60	10	10	10	8	9	13	**60**	60	10	10	12	8	10	10	**60**	60	8	10	11	8	10	13	**60**	**180**	180

List of Modules

RF bootcamp – **Prof. Marco Spirito**

Satellite Remote Sensing: open challenges and opportunities – **Prof. Giuseppe Ruello**

System on chip – **Prof. Nicola Petra**

Elettromagnetismo e relatività – **Prof. Amedeo Capozzoli**

Design of electronic circuits and systems – **Prof. Andrea Irace**

Cooperations

Politecnico di Milano

Prof. *Lorenzo Codecasa*

Kyoto University

Prof. *Alberto Castellazzi*

Qorvo Inc. (USA)

Dr. Peter J. Zampardi & Dr. Brian Moser

Primes innovation labs. (FRA)

Dr. Philippe Lasserre & Dr. Cyrille Duchesne

Period abroad

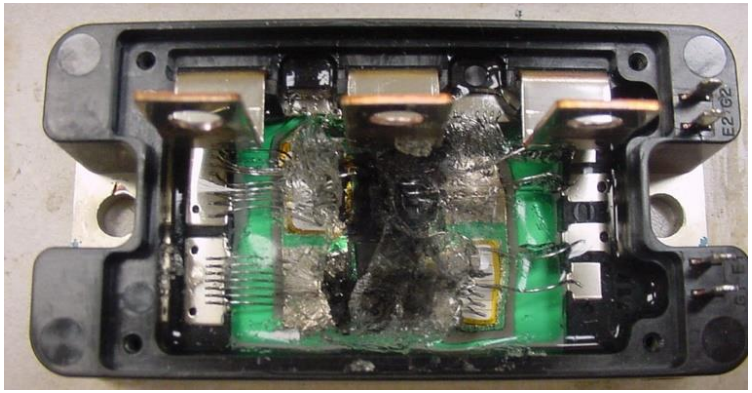
- February 1st – July 31st, 2019 (**6 months**)
- Prof. **Alberto Castellazzi**
- **PEMC group** – Power electronics and machine control
- **Thermal effects** in power electronics

The University of Nottingham

Motivations (1)

Self-heating effects:

- Variation of **electrical performances**
- Long-term **reliability reduction**
- Irreversible device and system **failure**

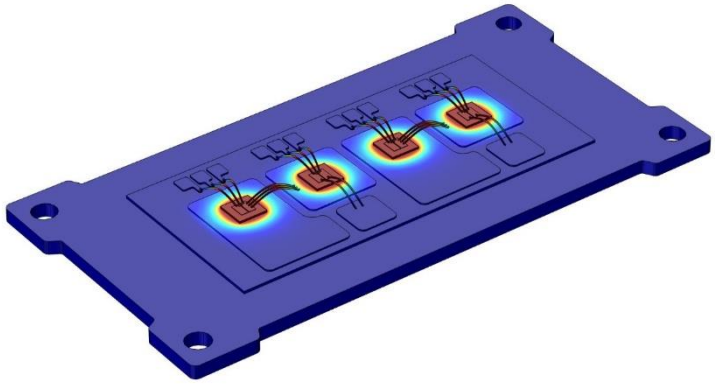


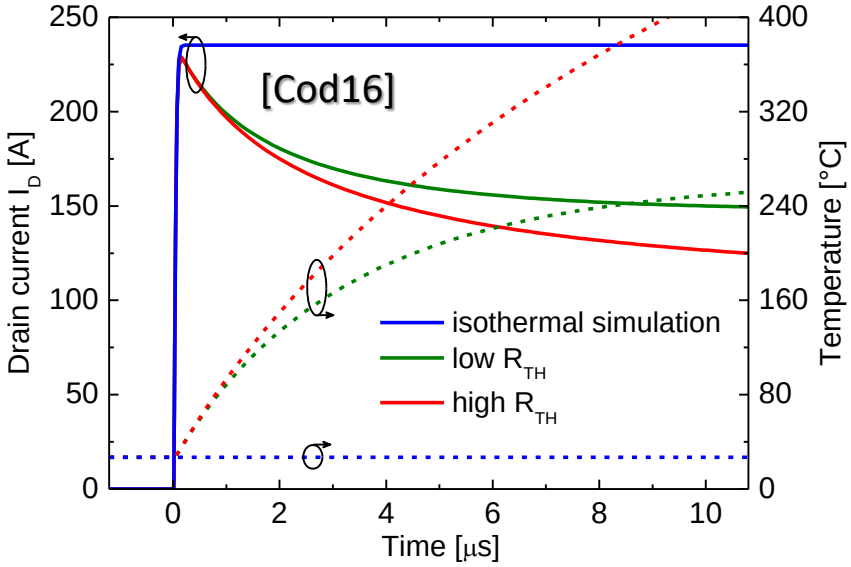
Thermal issues are the **main bottleneck** in many fields of **electronics**

Motivations (2)

Thermal simulations:

- Estimate the thermal behavior (R_{TH})
- Support the thermal design





Electrothermal simulations:

- Predict the true circuit performances
- Study instability effects

Research topics – RF devices

Heterojunction bipolar transistors (**HBTs**)

State-of-the-art devices

☺ high **cut-off frequency**

☺ high **current gain**

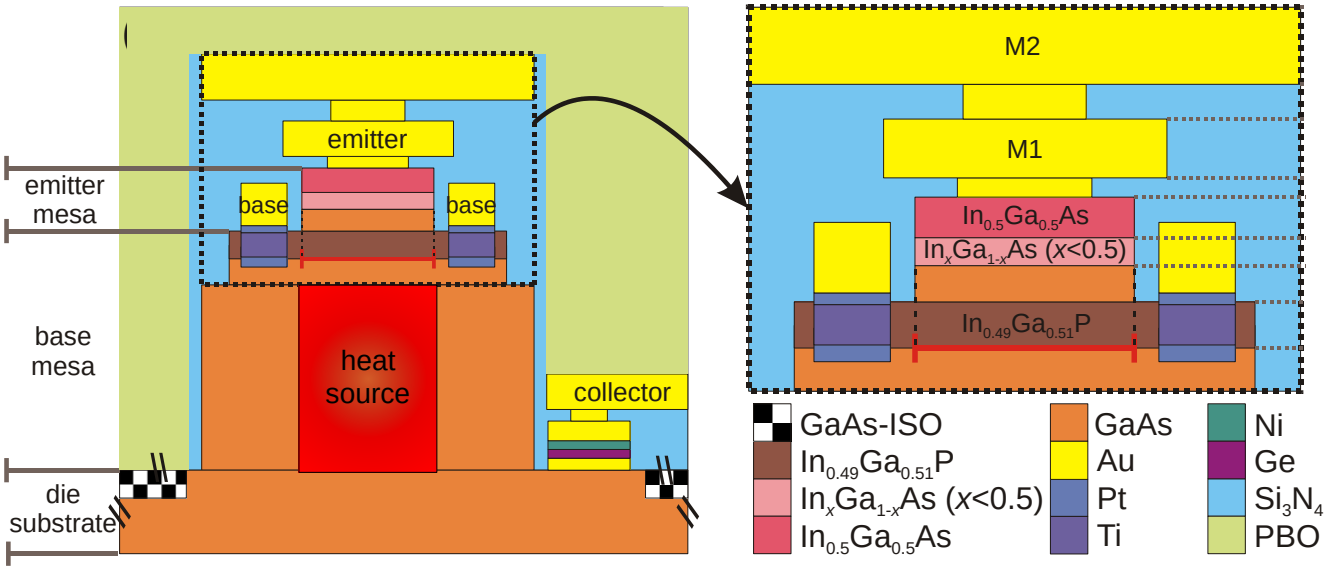
☹ Plagued by **thermal and electrothermal effects**

Contributions of my research activity:

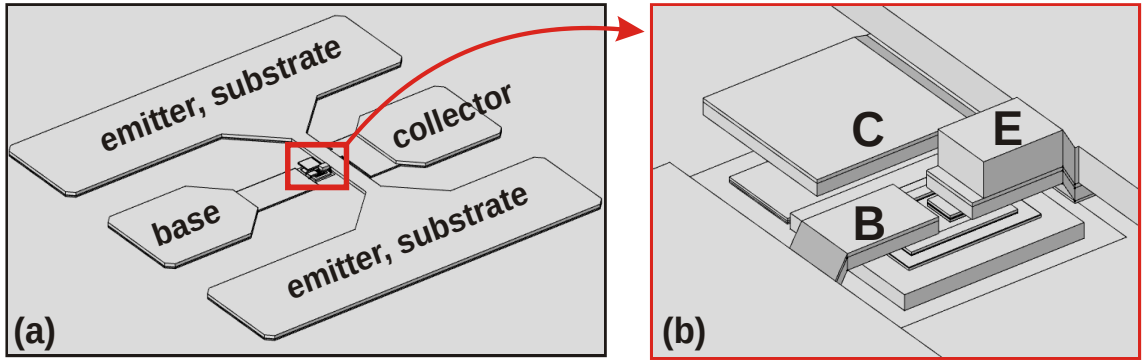
- Impact of **semiconductor and metal layers**
- Comparison between **packaging technologies**
- Steady-state **electrothermal behavior** of **arrays** of HBT

HBT Technology

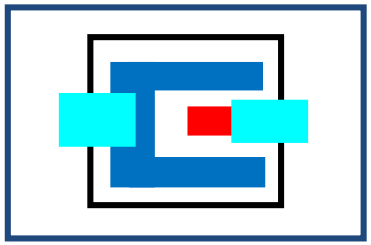
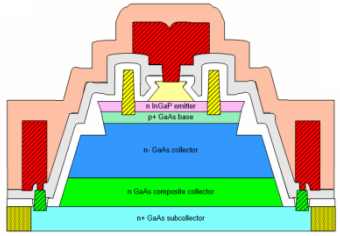
Mesa-isolated NPN transistors

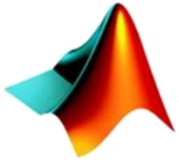


- **Semiconductor** layers suffer from **low thermal conductivity**!
- **Metallization** (in Au) promotes **heat shunt and spread** effects



Routine for FEM thermal simulations

Layout (.gds)  **+**  **Technology**

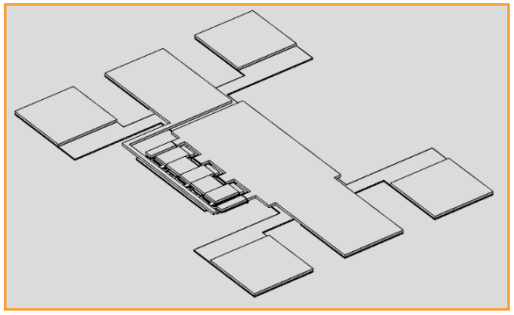


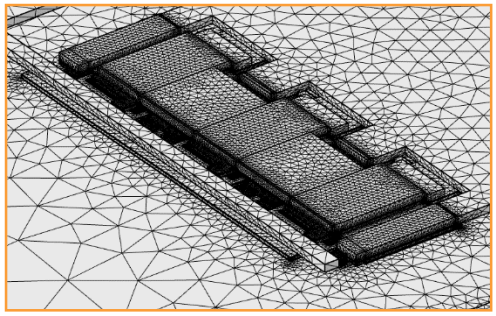
MATLAB

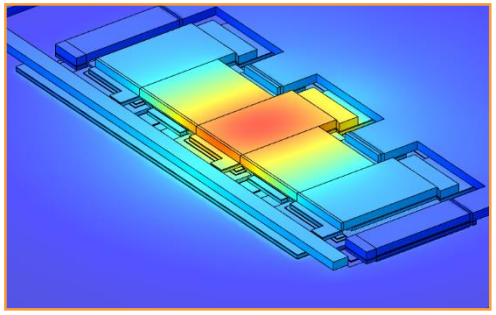
Automatically

COMSOL MULTIPHYSICS®

Geometry **+** **Meshing** **+** **Solution**



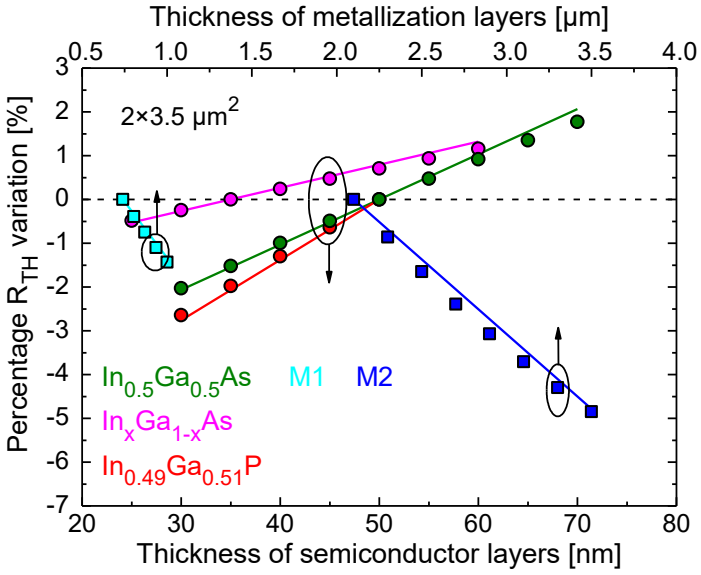




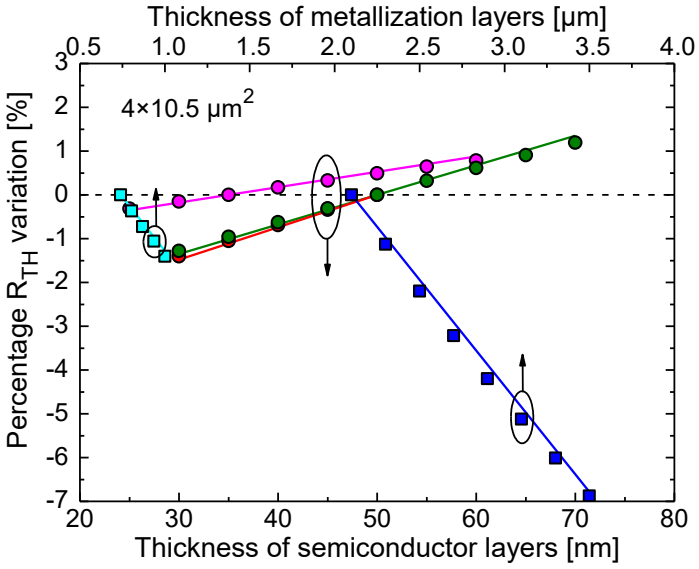
Extremely detailed structures for highly accurate simulations [dAl17]

Impact of semiconductor and metal layers

- The analyses allow **quantifying the impact** of each layer of interest on the **device R_{TH}**
- **Design of experiments (DOE)** technique was exploited to build **analytical models** for the R_{TH} estimation



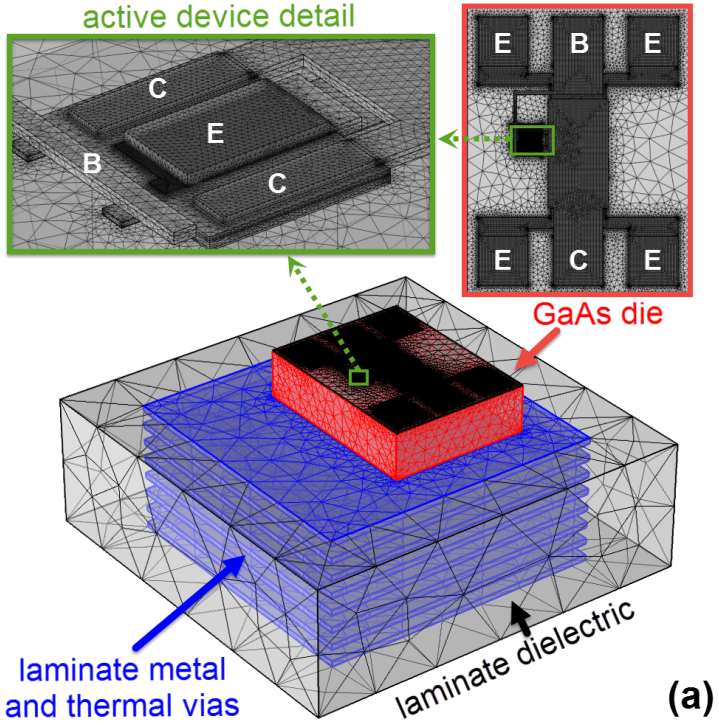
Small-emitter HBT

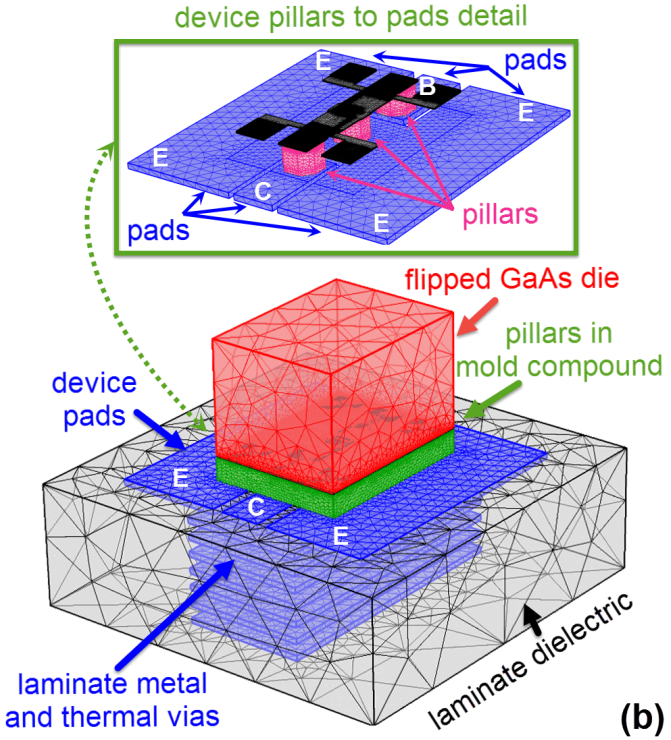


Big-emitter HBT

Packaging technology (1)

Thermal comparison between wire-bonding and flip-chip packaging including the effect of laminate



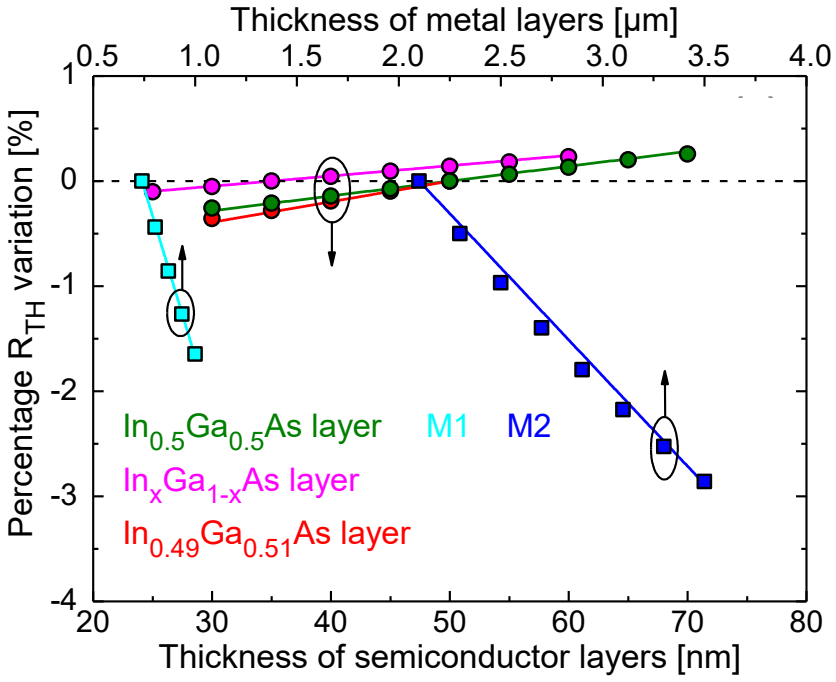


Wire-bonding

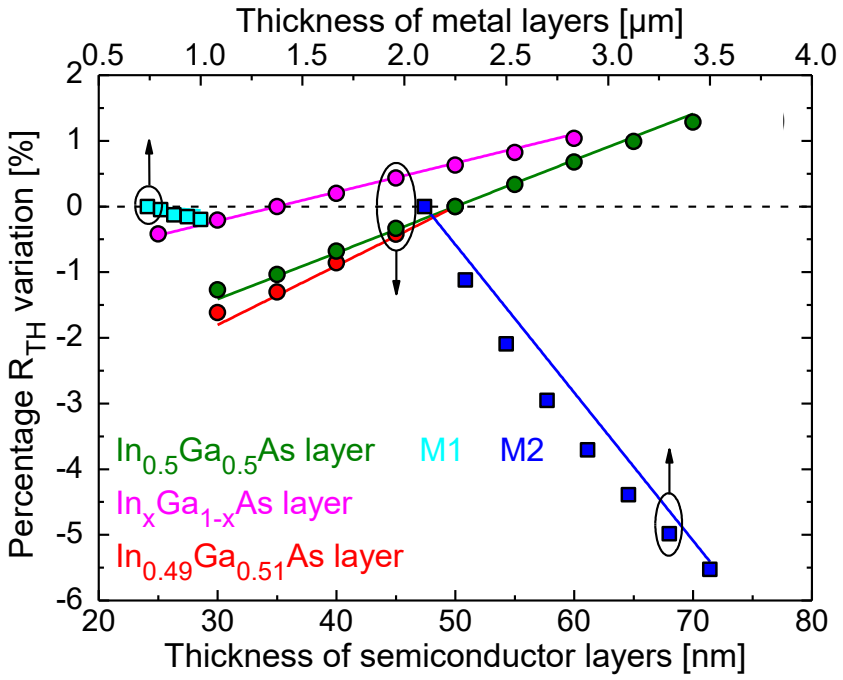
Flip-chip

Packaging technology (2)

Wire-bonding $R_{THref} = 421.7$ K/W

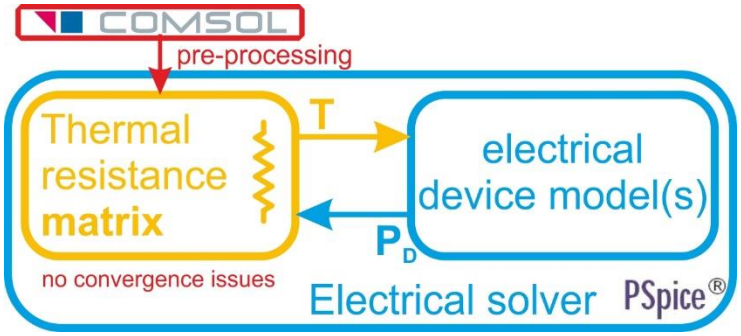


Flip-chip $R_{THref} = 240.6$ K/W

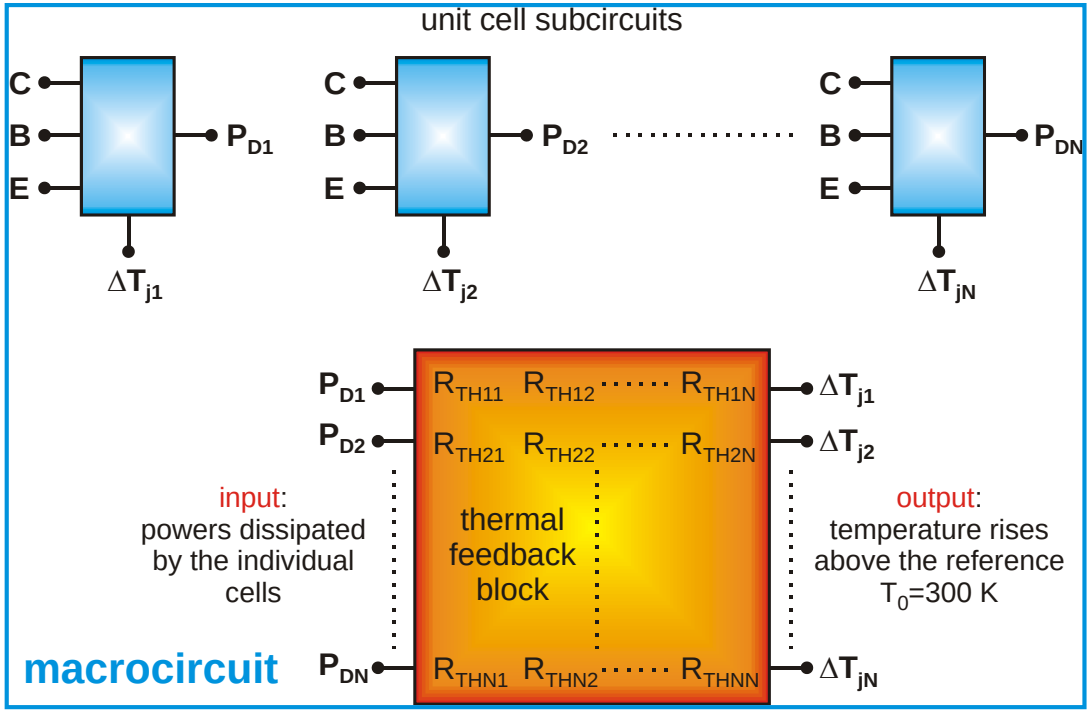


- DOE-based evaluation of the **layers of interest** in both technologies
- Impact of **laminate** on the heat **shunt and spread** mechanisms

Steady-state ET analyses



Electrothermal simulations based on **compact thermal model**

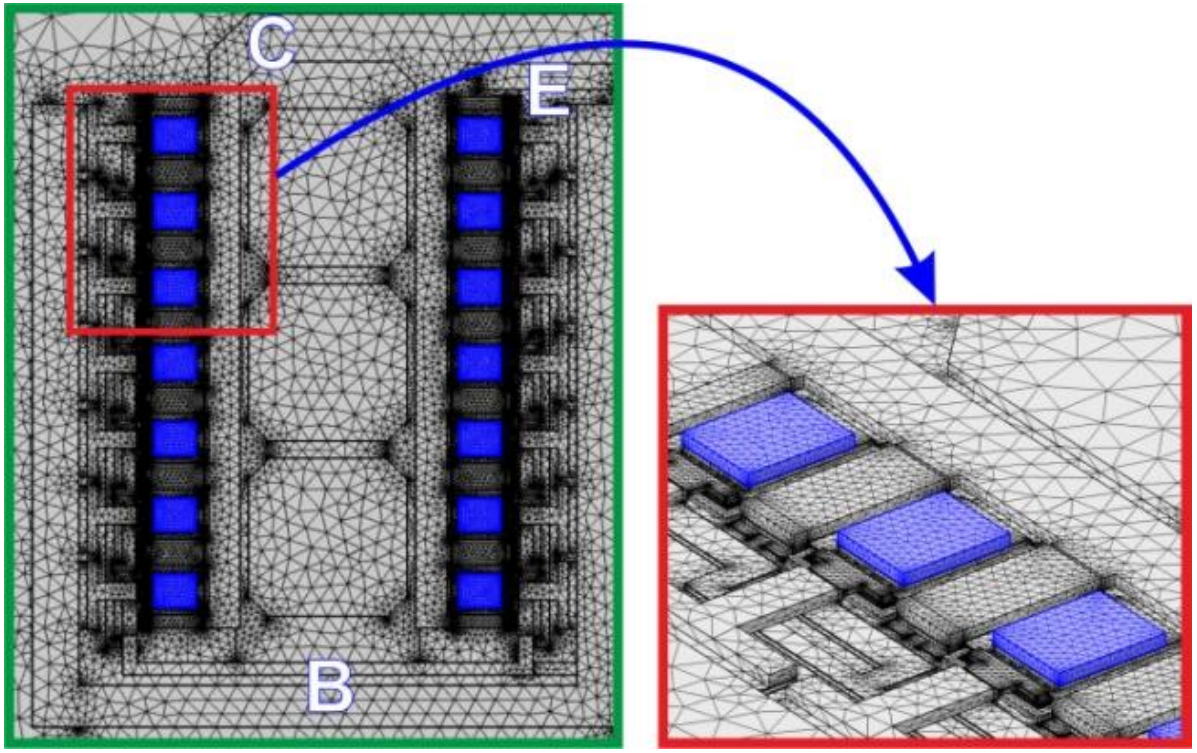


Electrical HBT model includes the **temperature dependences of the electrical parameters**

Accurate yet fast electrothermal simulations

Steady-state ET analyses

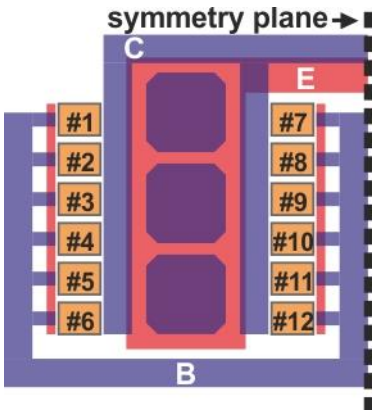
HBT arrays composed of 24 or 28 unit cells

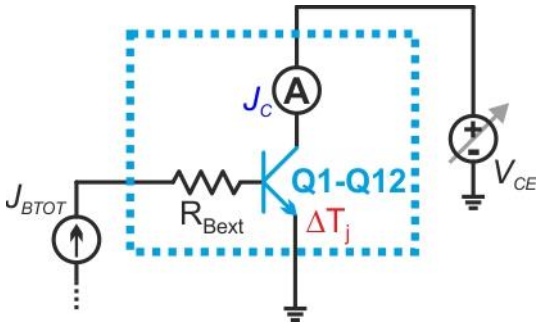


Steady-state ET analyses

24-cell array

Even number of cells (6) per column

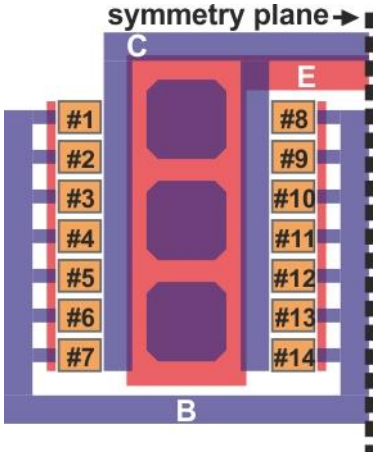


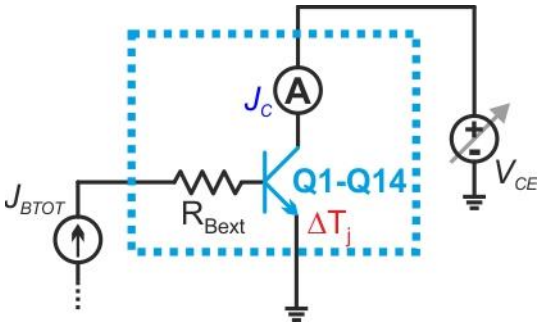


VS

28-cell array

Odd number of cells (7) per column

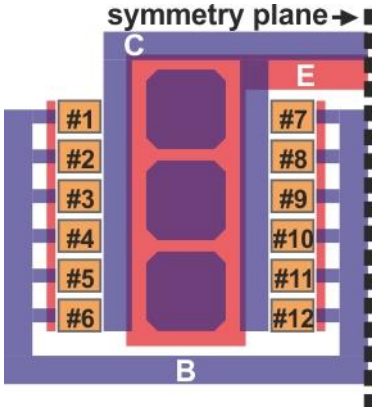


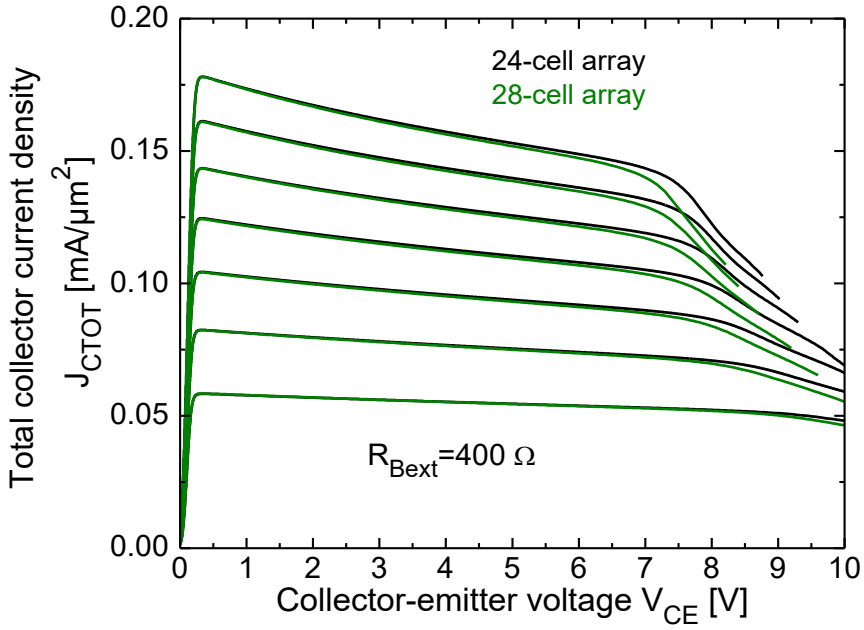


Steady-state ET analyses

24-cell array

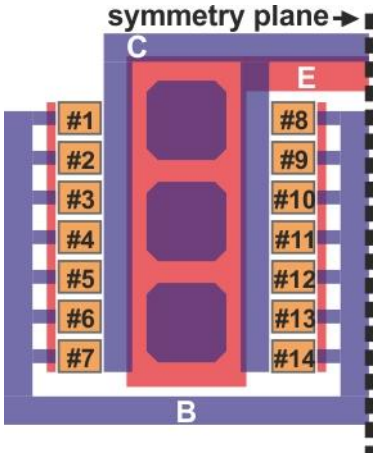
Even number of cells (6) per column

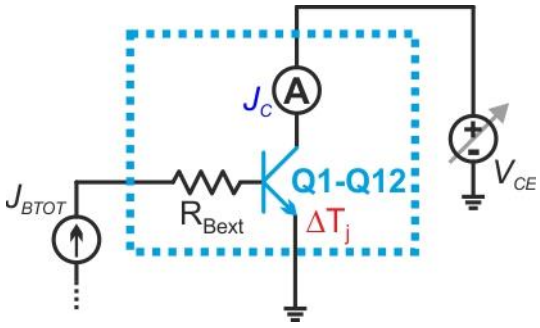




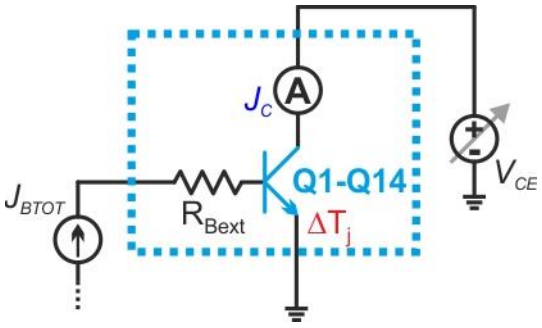
28-cell array

Odd number of cells (7) per column





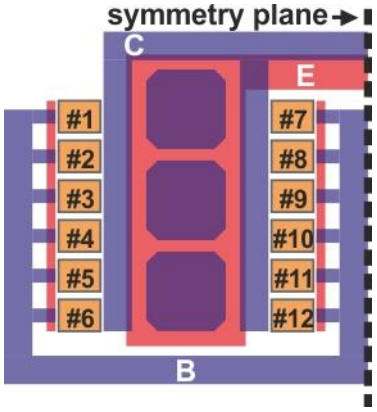
The **collapse of current gain** occurs at higher V_{CE} for 24-cell array: two cells (#9 and #10) concurrently share I_{CTOT} in the **24-cell array**; it is conducted only by one cell (#11) in the **28-cell array.**

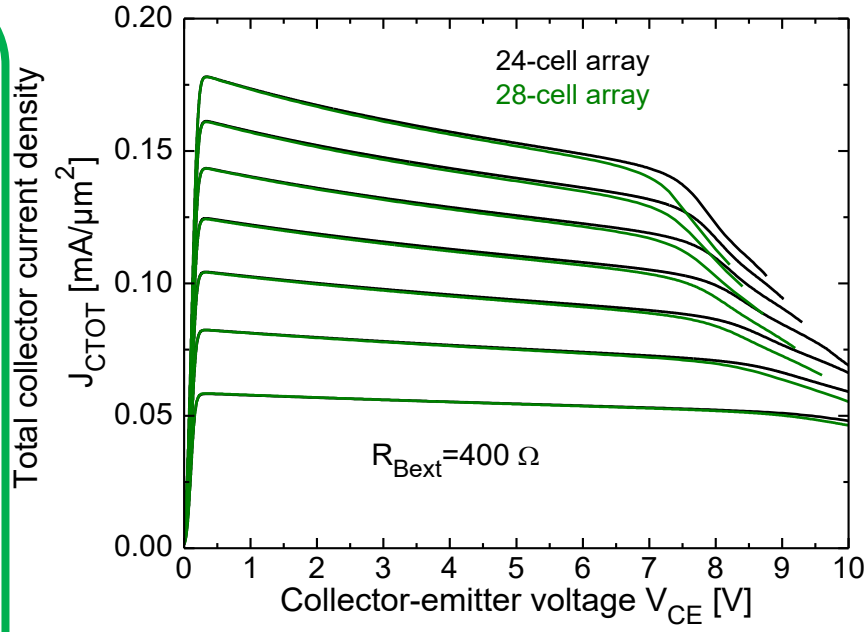


Steady-state ET analyses

24-cell array

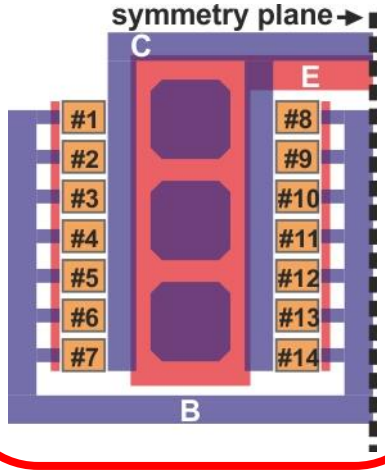
Even number of cells (6) per column





28-cell array

Odd number of cells (7) per column



The **collapse of current gain** occurs at higher V_{CE} for 24-cell array: two cells (#9 and #10) concurrently share I_{CTOT} in the **24-cell array**; it is conducted only by one cell (#11) in the **28-cell array.**

WINNER

LOSER

Research topics – Power systems

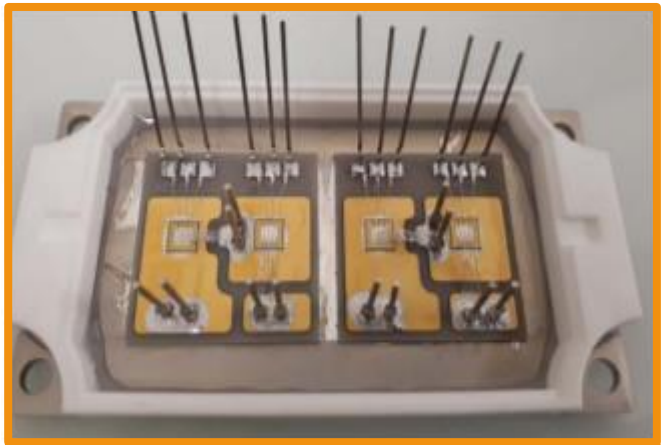
SiC-based MOSFETs on **power modules**:

- **Single- and double-sided cooled** technologies
- Effects of **technology fluctuations** on the ET behavior of power circuits

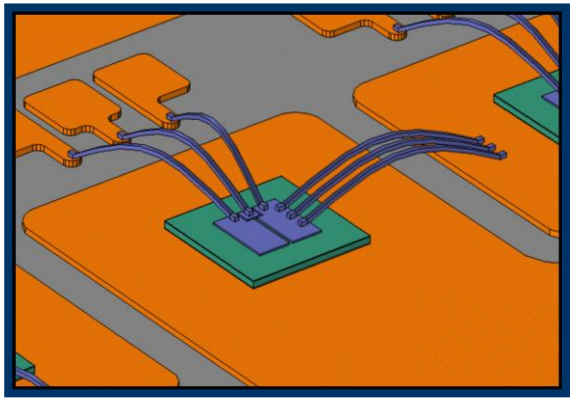
GaN-based HEMTs on **PCB**:

- **Analytical models** supporting the thermal design
- **Simulations and experiments** for the evaluation of the **models accuracy**

SSC vs DSC power modules (1)

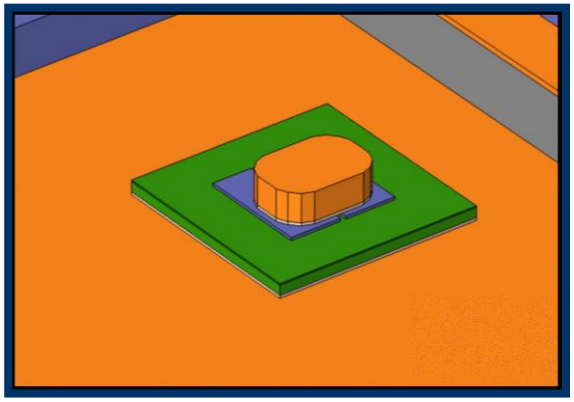


SINGLE-SIDED COOLED POWER MODULE



bond wires

DOUBLE-SIDED COOLED POWER MODULE



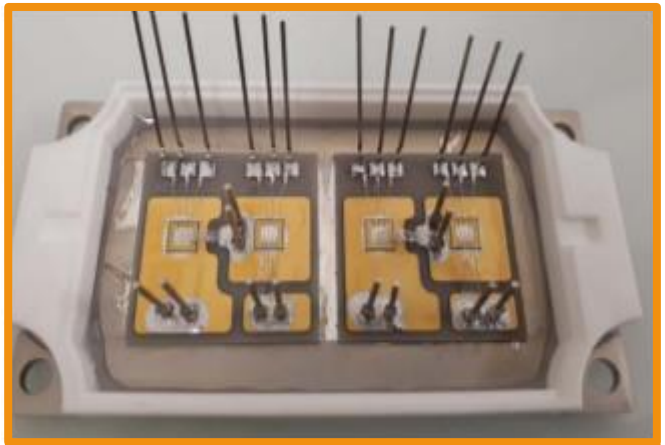
bumps

☺ low parasitics

☺ compactness

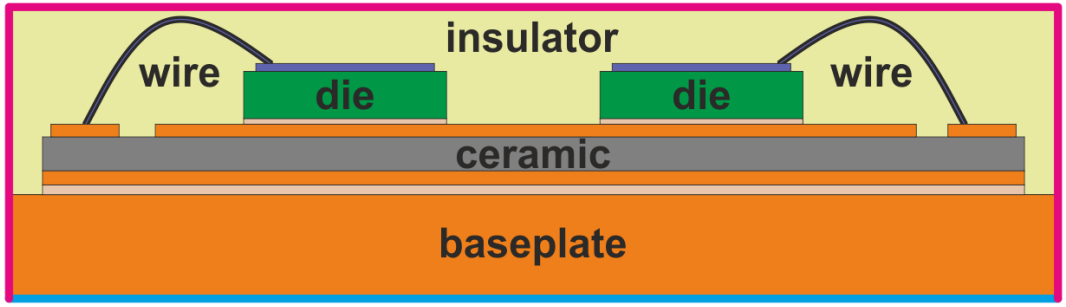
☹ higher costs

SSC vs DSC power modules (1)

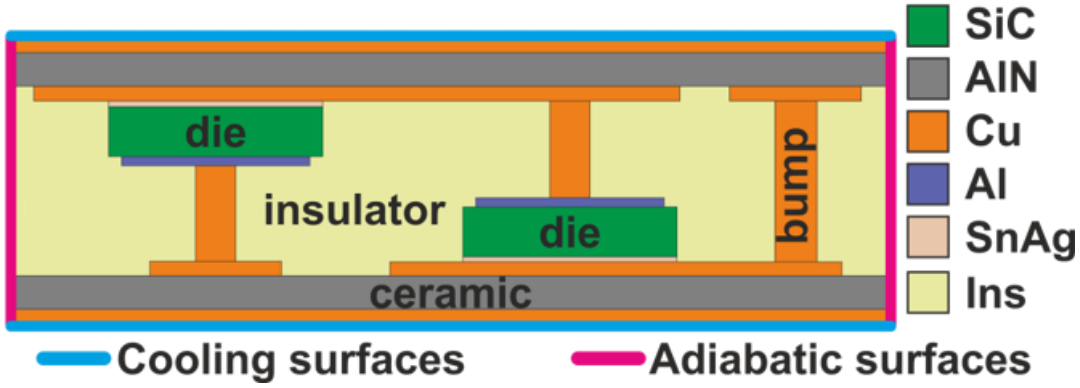


SINGLE-SIDED COOLED
POWER MODULE

1 cooling surface



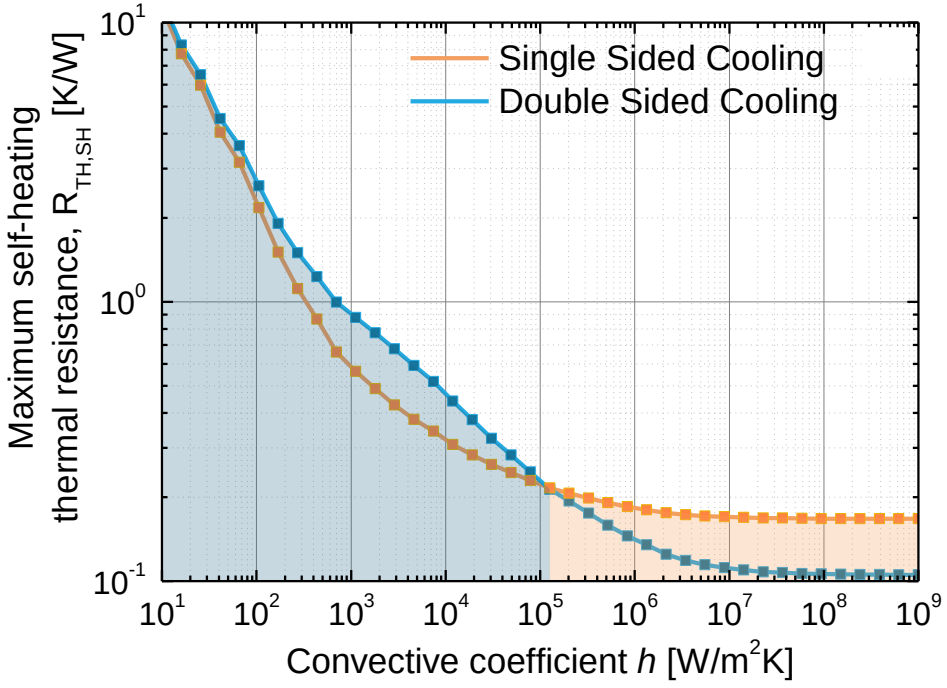
DOUBLE-SIDED COOLED
POWER MODULE



2 cooling surfaces

SSC vs DSC power modules (2)

$R_{THmax,Self-Heating}$



😐 **DSC does not offer better self-heating R_{TH}** for every boundary condition

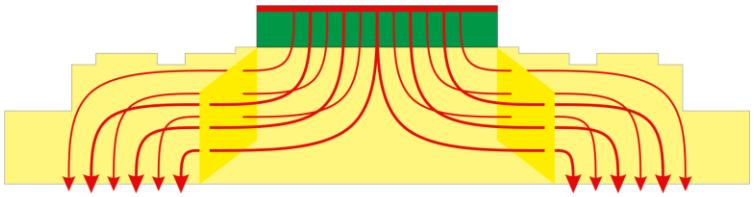
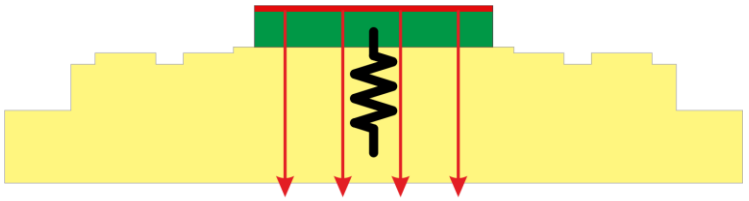
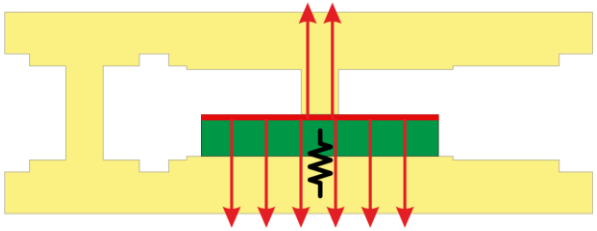
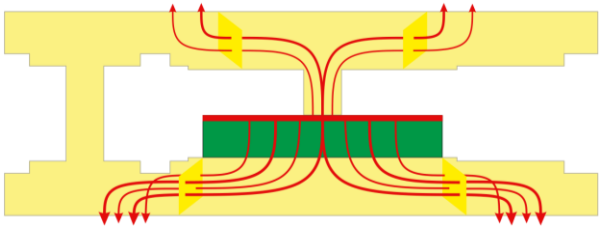
😐 An h value ($h_{TR} \approx 10^5$ W/m^{2}K) determines a **trend reversal behavior**

☹ $h < h_{TR}$ → the SSC is cooler than the DSC

☺ $h > h_{TR}$ → the DSC is cooler than the SSC

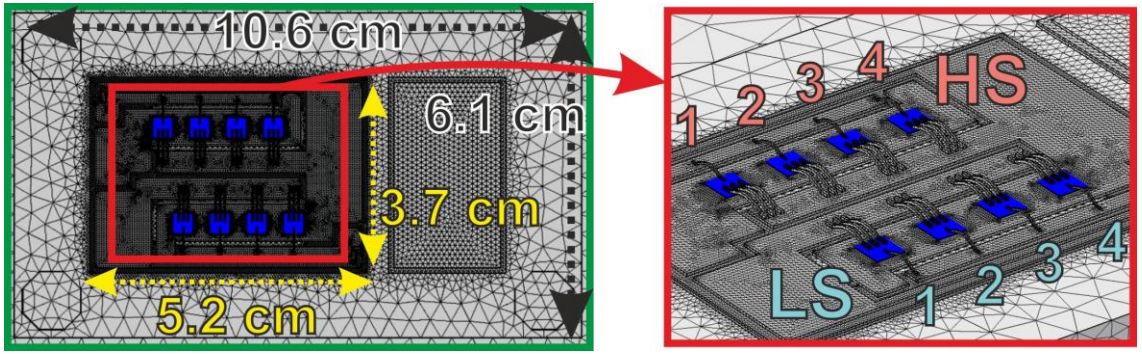
HOW CAN WE EXPLAIN THIS BEHAVIOR?

SSC vs DSC power modules (3)

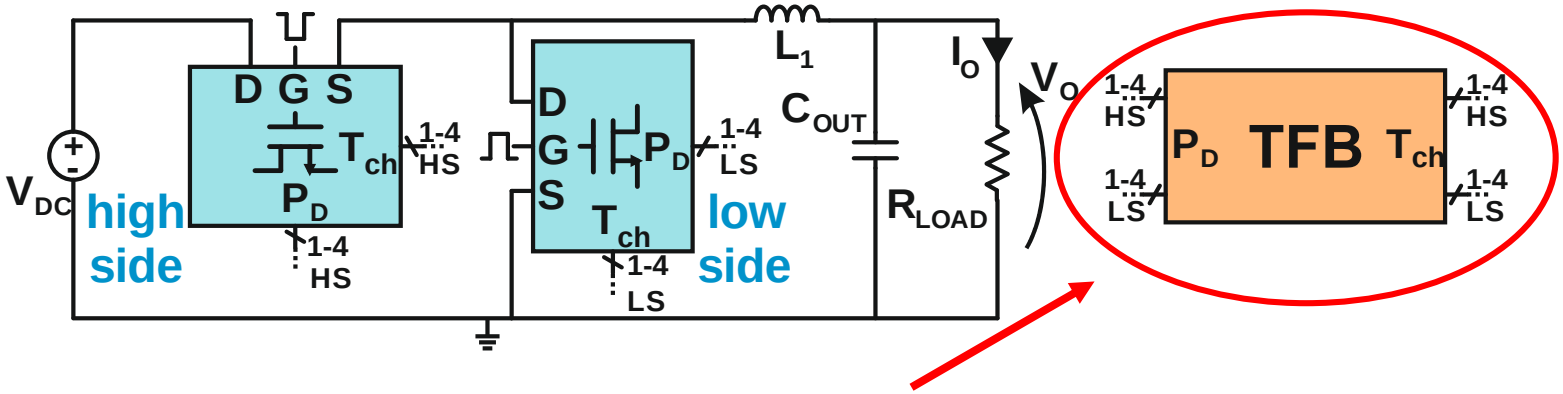
	Advantages ☺	Disadvantages ☹
SSC	**High spread** through the thick baseplate 	**High thermal resistive path** between HS and CS **because of the baseplate** 
DSC	Low thermal resistive path between HS and CS because of the **two cooling surfaces** 	**Low spread** through the **thin DBCs** 

The **DSC** is convenient only in presence of a **good cooling system**

SiC MOSFET technology fluctuation



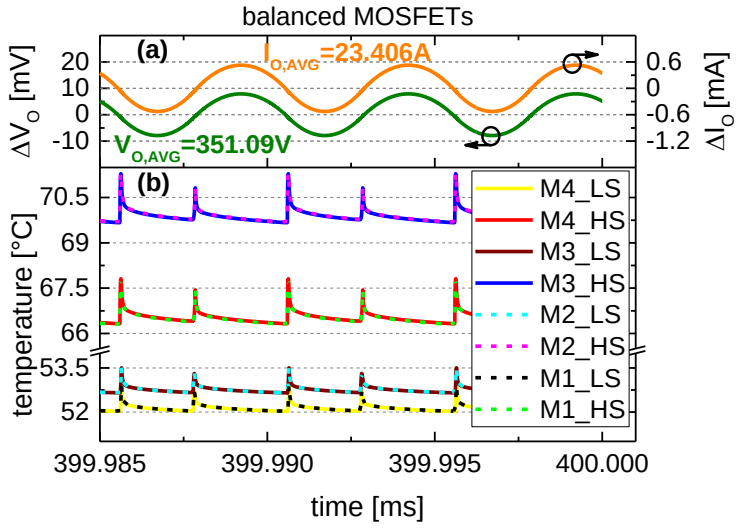
SSC PM with **half bridge** circuit
4 MOSFETs per side



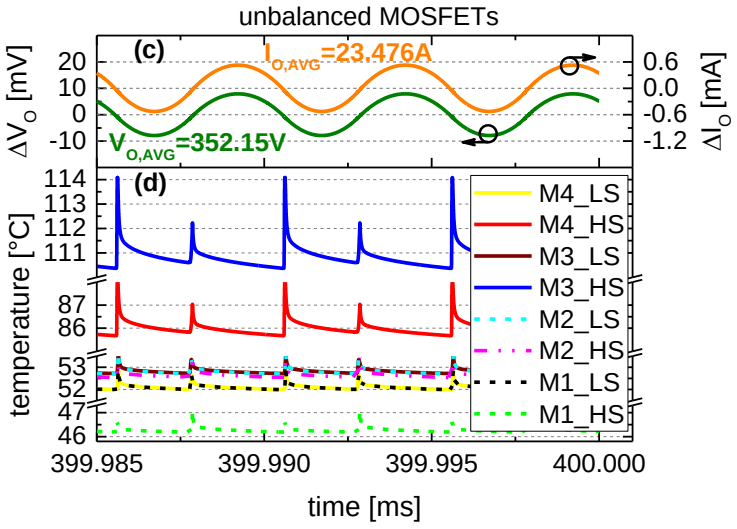
Obtained by **model-order reduction** approach

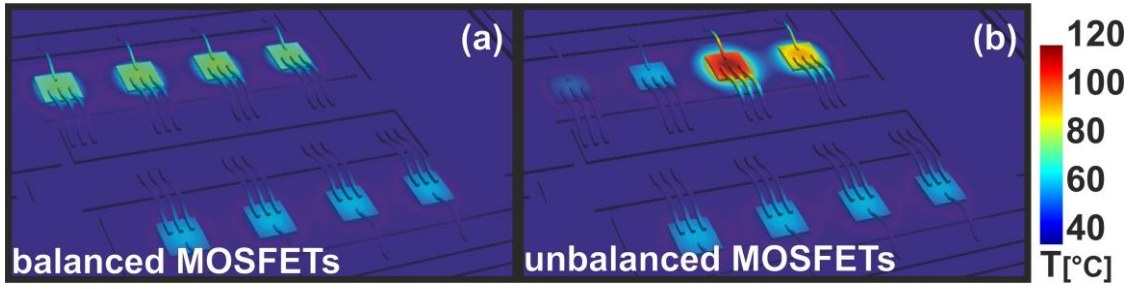
SiC MOSFET technology fluctuation

Balanced MOSFETs



Unbalanced MOSFETs





It is **hard to recognize** technology fluctuations from the **PM terminals**

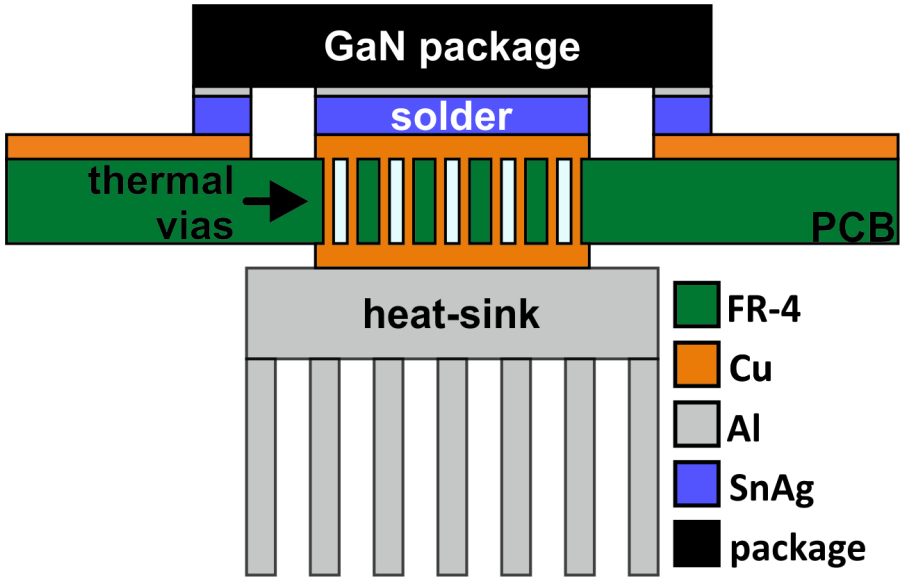
Technology fluctuations **strongly affect** the long-term **reliability**

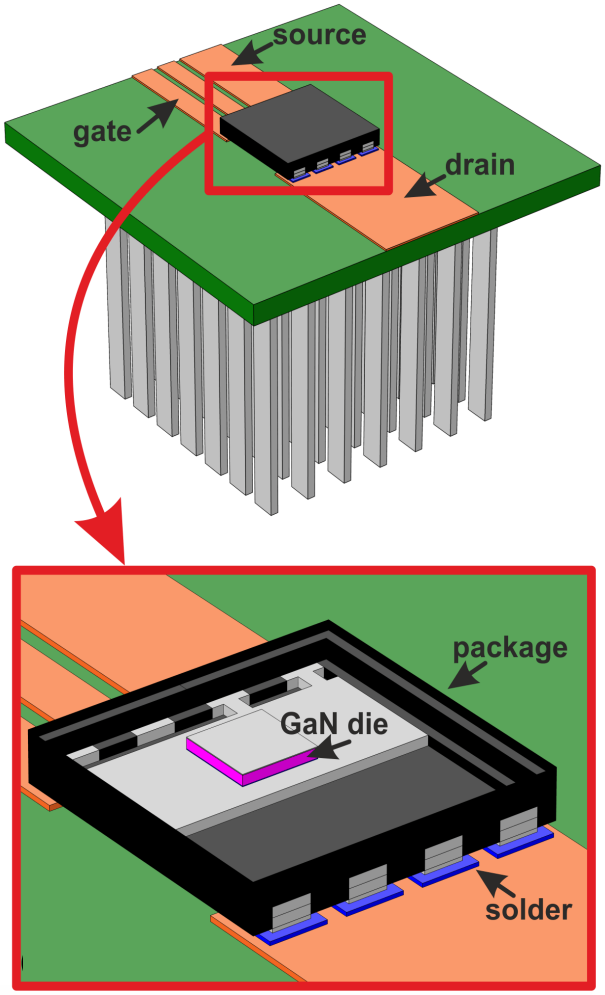
Thermal models of PCB cooling solutions

Thermal PCB design **is necessary**

It usually requires:

- Experimental characterization
- Skills in numerical simulations





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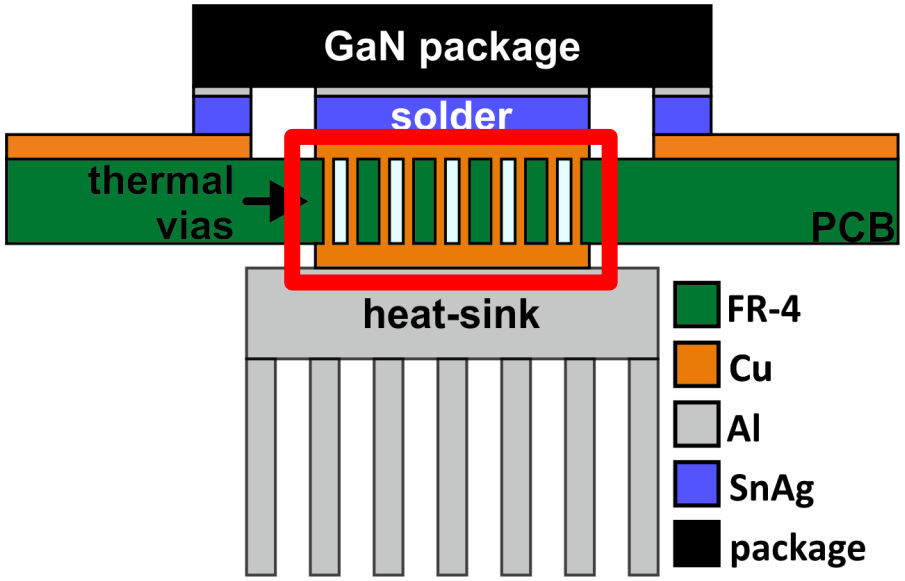

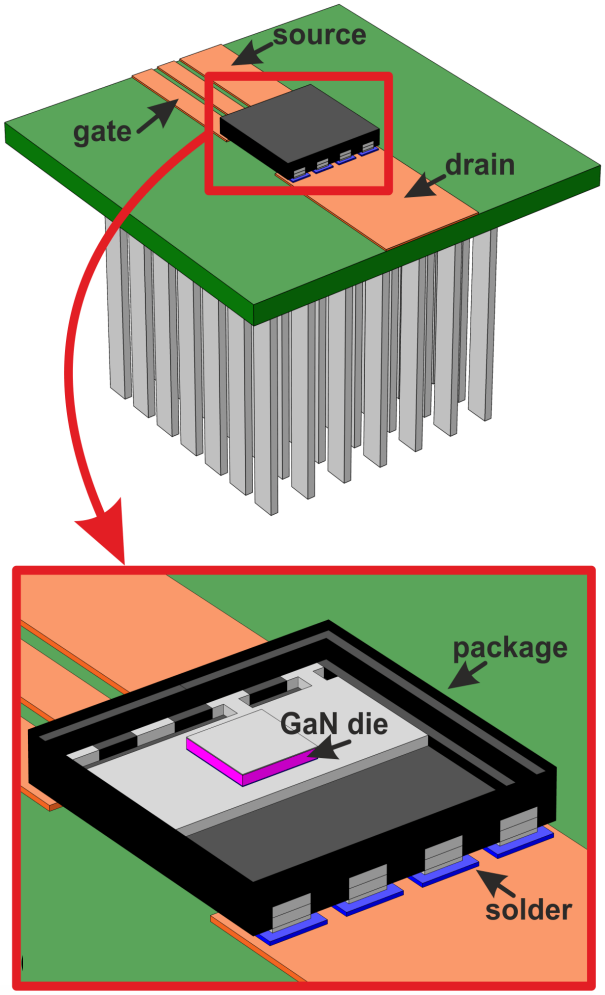

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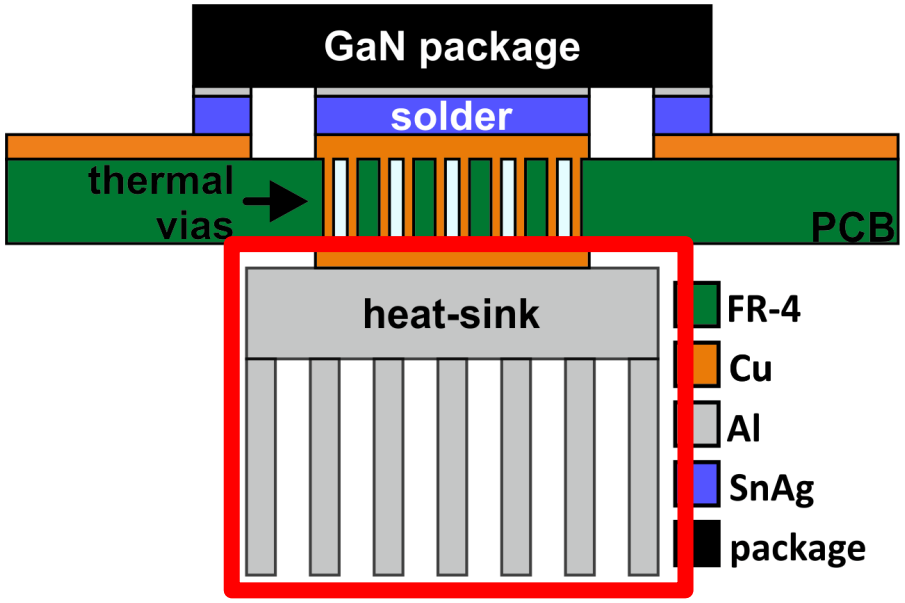
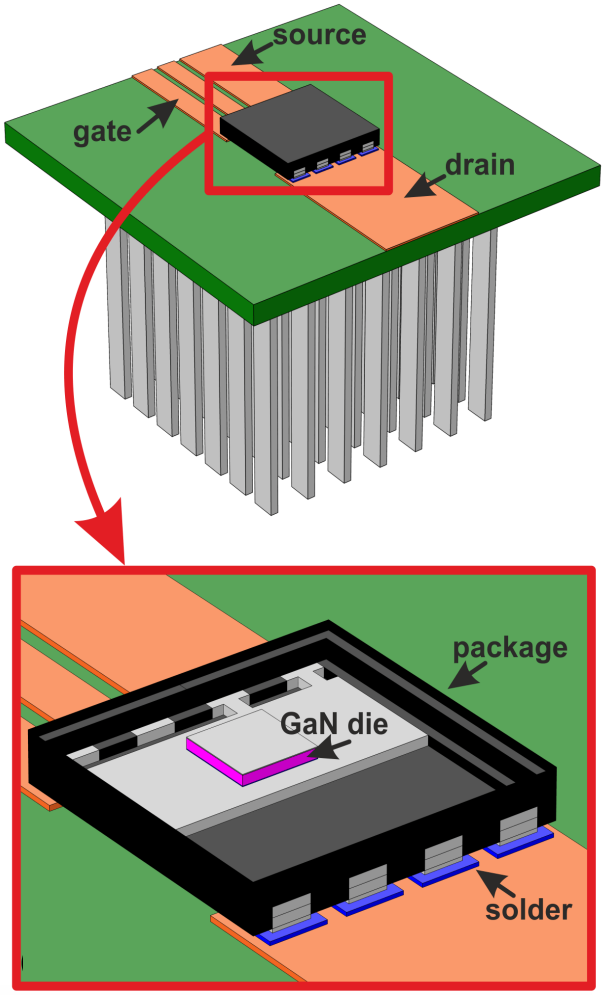
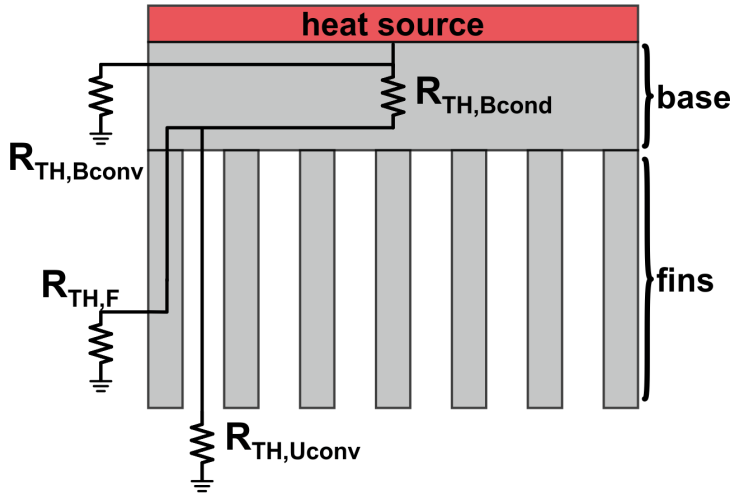


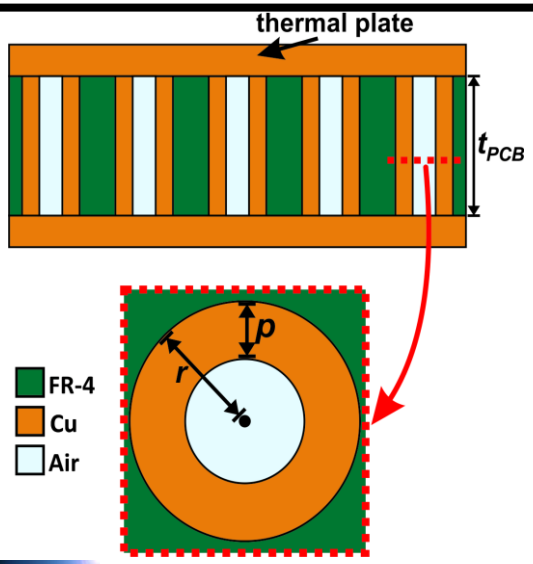


Thermal models of PCB cooling solutions

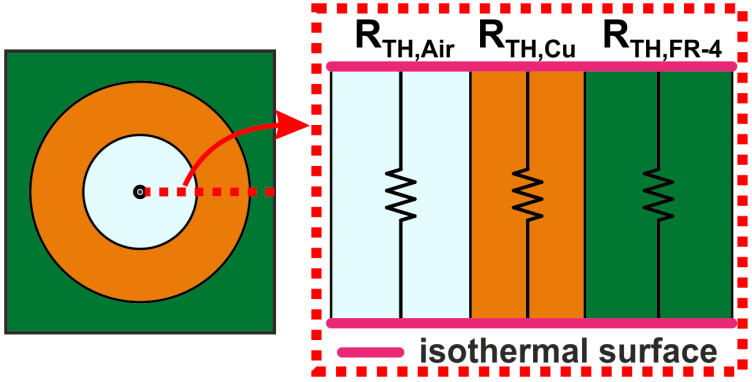
$$R_{TH,HSK} = \left[R_{TH,Bcond} + (R_{TH,Uconv} \,//\, R_{THtot,F}) \right] // \, R_{TH,Bconv} =$$

$$= \left[R_{TH,Bcond} + (R_{TH,Uconv} \,//\, \frac{R_{TH,F}}{N_{Fin}}) \right] // \, R_{TH,Bconv}$$

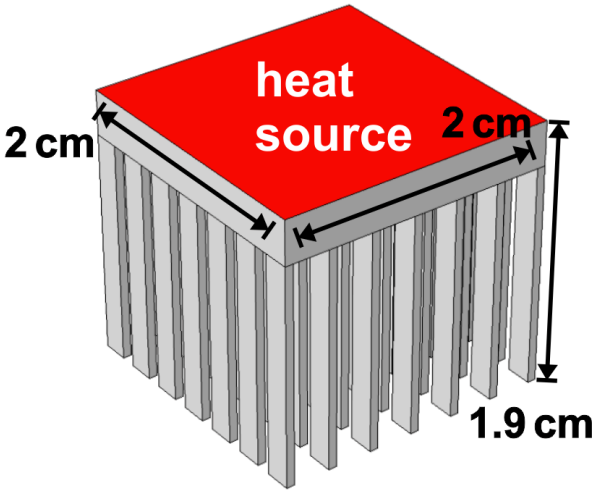




$$R_{TH,TV} = R_{THtot,Cu} \,//\, R_{THtot,FR-4} \,//\, R_{THtot,Air}$$



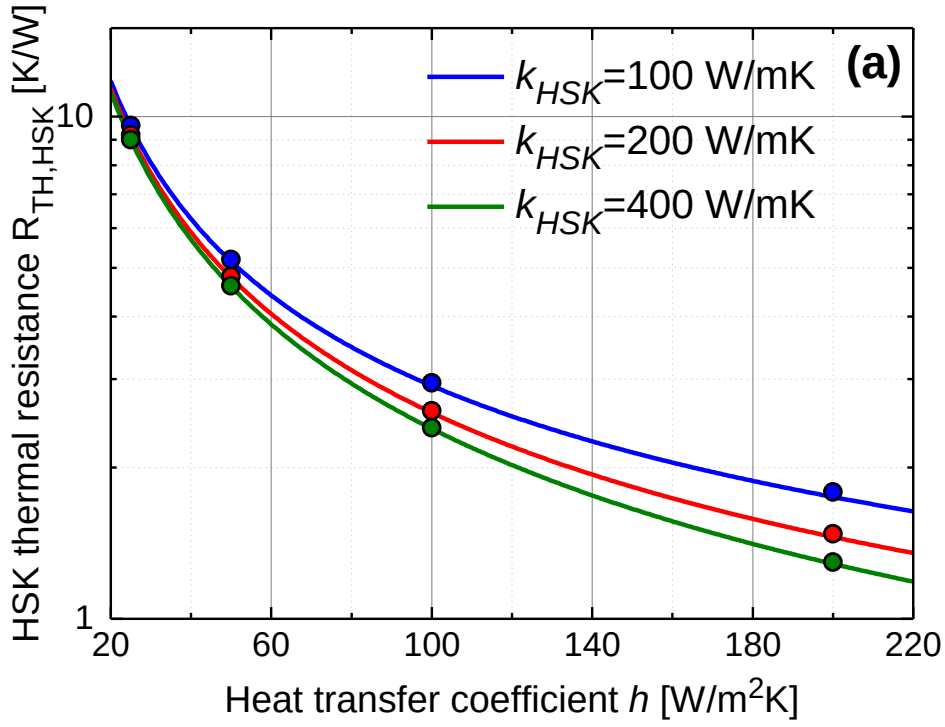
Thermal models of PCB cooling solutions



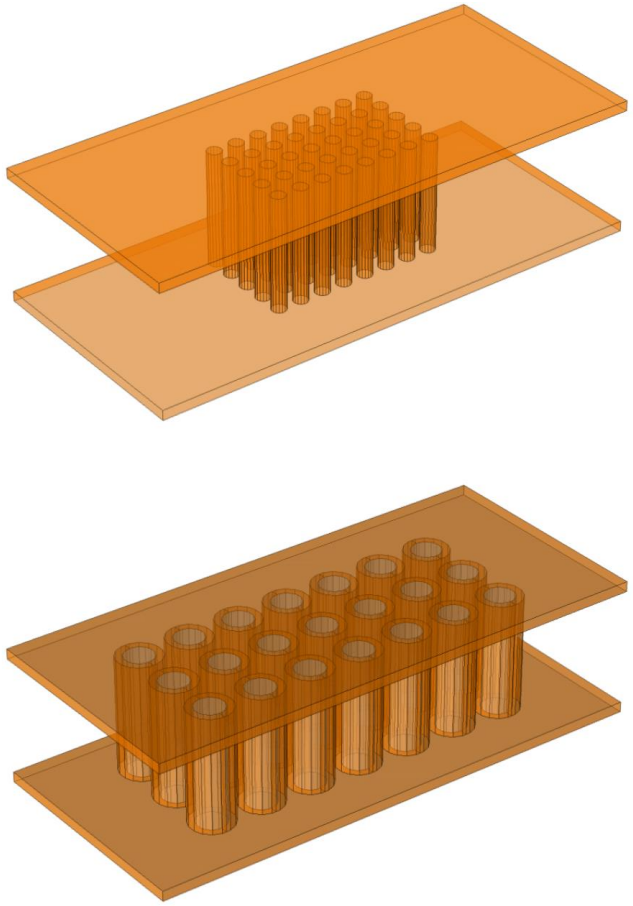
HSK for **single-device** application with **7 × 7 rectangular fins.**

Validated in a **wide-range of convective coefficients** *h* and for **3 thermal conductivity** *k* values

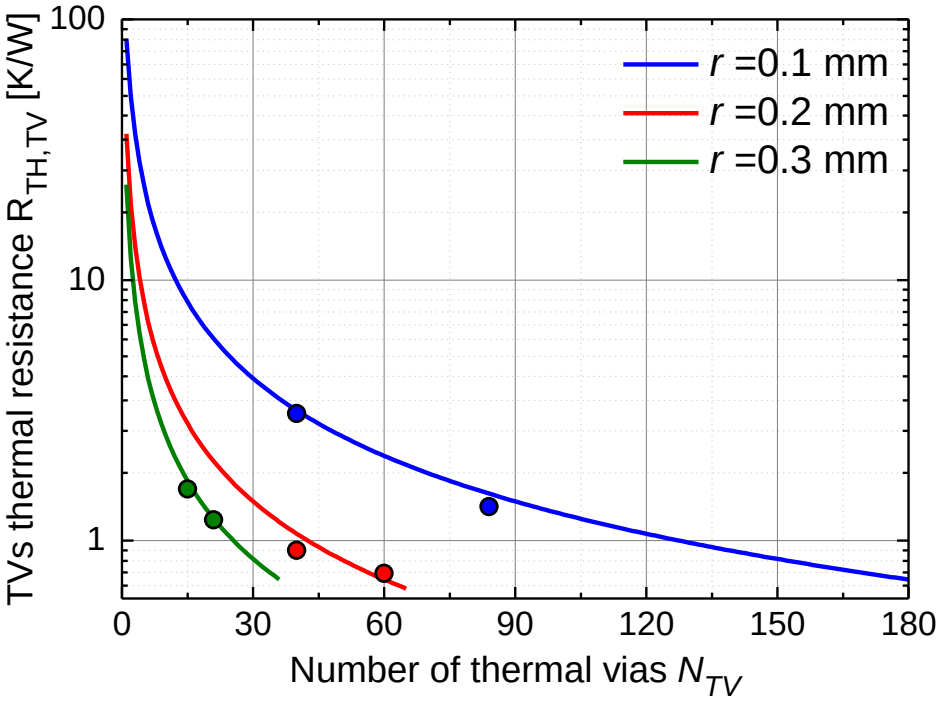
Maximum error → **less than 1%**



Thermal models of PCB cooling solutions



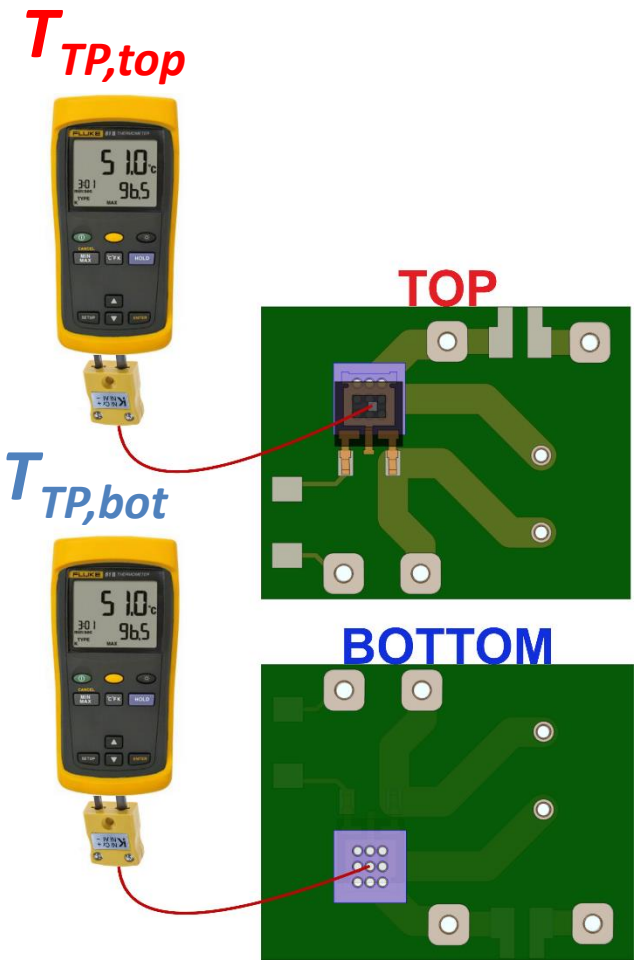
- **3.2 × 7 mm²**-wide thermal plates
- Validated for **0.1mm** of plating
- **6 TVs design** were studied



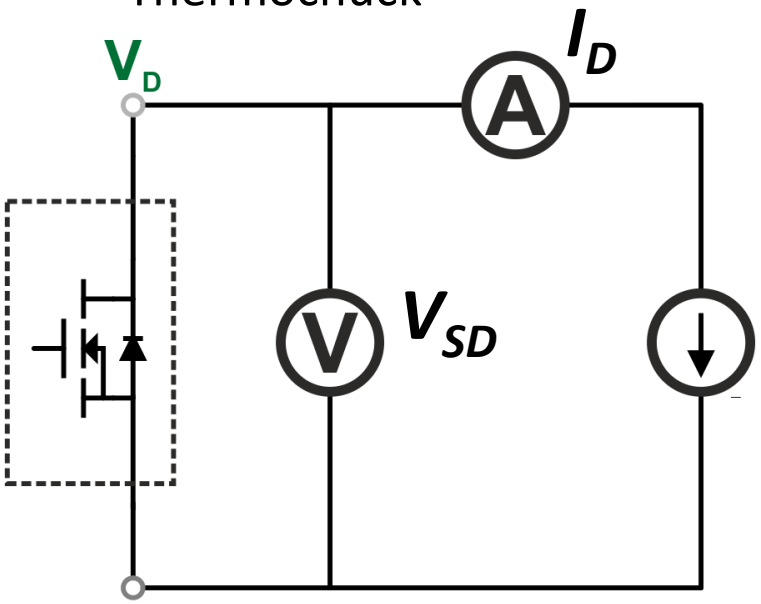
Average discrepancy of **5.8%**

Thermal models of PCB cooling solutions

Experimental setup



- #2 Thermocouples
- Current generator
- Current and voltage probes
- Thermochuck



$$R_{TH,TV} = \frac{T_{TP,top} - T_{TP,bot}}{I_D V_{SD}}$$

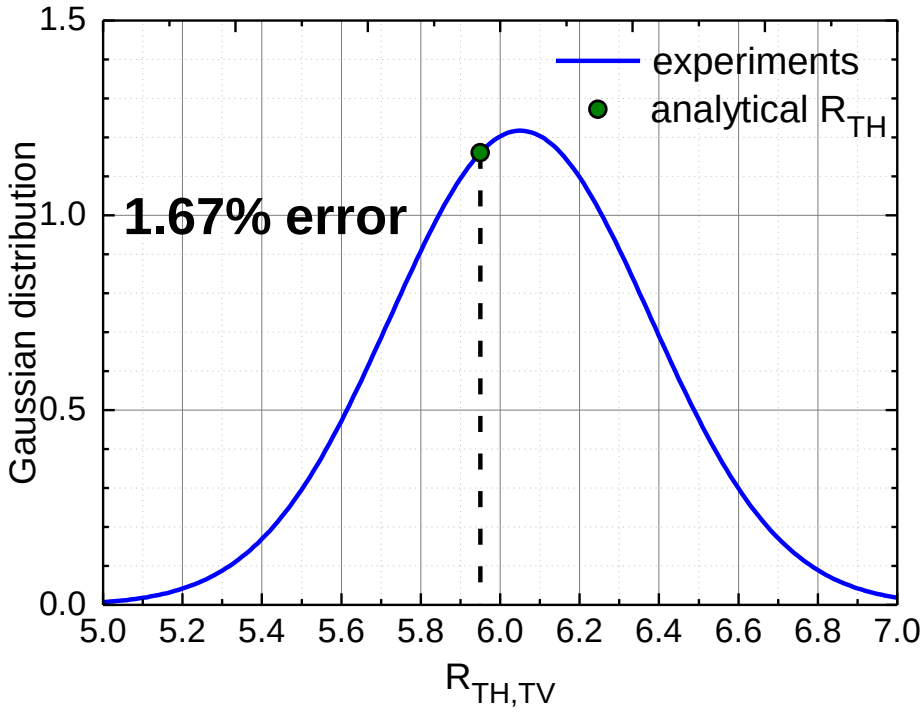
Thermal models of PCB cooling solutions

20 Experiments:

0.5A < $\mathbf{I_D}$ < 3A

0.65V < $\mathbf{V_{SD}}$ < 0.75V

0.33W < $\mathbf{P_D}$ < 2.25W



Model **accuracy** is also verified by **experiments**

Publications and presentations

Journal papers: **3**

Conference papers: **17** (12 of which on **IEEE Xplore**)

Contributions in **book series**: **3**

Scopus ***h-index*** (on Feb 1st, 2020) : **4**

Oral presentations: **6** (1 of which as **Keynote**)

Poster presentations: **4**

I have **backup slides** for **further results** of my research activity

Thank you for your kind attention.