



**PhD in Information Technology and Electrical Engineering**

**Università degli Studi di Napoli Federico II**

**PhD Student: Antonio Pio Catalano**

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**XXXII Cycle**

**Training and Research Activities Report – Third Year**

**Tutor: Prof. Vincenzo d'Alessandro**



# Training and Research Activities Report – Third Year

PhD in Information Technology and Electrical Engineering – XXXII Cycle

Antonio Pio Catalano

## 1. Information

I received the M. Sc. Degree, cum laude, in Electronic Engineering from University of Napoli ‘Federico II’ in October 27<sup>th</sup> 2016 with the thesis “*Numerical Optimization of GaAs HBT Thermal Ruggedness with Design Of Experiments*”. I belong to XXXII cycle of Information Technology and Electrical Engineering (ITEE) PhD. My fellowship is financed by athenaeum. My tutor is Prof. Vincenzo d’Alessandro.

## 2. Study and Training activities

Study and training activities are summarized below:

### a. Modules

- Design of electronic circuits and systems – Prof. Andrea

### b. Seminars

- Robots in medical applications: an overview of the current medical robotics market from industry’s point of view - Dott. Schettino
- Medical thermal therapy and monitoring using microwave inverse scattering - Prof. Moehaddam
- DESIGN MATTER: meta-material interaction with light, radiowaves and sound - Prof. Alù
- Ethics, Science and Society in brain computer interface - Prof. Haselager
- Lo spazio cibernetico come dominio bellico - Dott. Siroli
- A Dynamic and probabilistic orienteering problem - Prof. Archetti
- Flexible two-echelon location-routing for supply networks - Prof. Archetti
- Deep learning onramp - Dott. Marrone

During the 3<sup>rd</sup> year I didn’t attend external courses.

Student: Antonio Pio Catalano <a href="mailto:antoniopio.catalano@unina.it">antoniopio.catalano@unina.it</a>								Tutor: Prof. Vincenzo d’Alessandro <a href="mailto:vindales@unina.it">vindales@unina.it</a>								Cycle XXXII											
Credits year 1								Credits year 2								Credits year 3											
	Estimated	1	2	3	4	5	6	Summary	Estimated	1	2	3	4	5	6	Summary	Estimated	1	2	3	4	5	6	Summary	Total	Check	
Modules	20	3	0	0	0	3	9	15	10	0	0	4	0	0	5	9	0	0	0	0	0	0	0	9	9	33	30-70
Seminars	5	1.9	0	0	3	0.8	0.3	6	5	0	0.4	0.5	0	0	0	0.9	0	0	0.8	0.5	0	2.1	0	3.4	10	10-30	
Research	35	5.1	10	10	5	5.2	3.7	39	45	10	9.6	7.5	8	10	5	50	60	8	9.2	11	8	7.9	4	48	137	80-140	
	60	10	10	10	8	9	13	60	60	10	10	12	8	10	10	60	60	8	10	11	8	10	13	60	180	180	

## 3. Research activity

My third year as PhD student started with the period abroad in ‘University of Nottingham (UK)’ followed by prof. Alberto Castellazzi. There, I applied the methodologies developed in the previous years to the topics of Power Electronics; the main categories of which are summarized in the following:

*SiC-based power modules* – The power modules represent a commercial solution to realize power circuits; since the active devices are embedded in such modules in a bare-die configuration, the modules are characterized by high rates in terms of both electrical and thermal behavior. The analyses carried out in this field are about a new technology of power modules denoted as Double-

Sided cooled (DSC), which is a good candidate to replace the classical technology (i.e., the single-sided cooled one).

A comparison in term of thermal behavior has been studied and published in a conference paper for the IEEE Thermnic 2019 workshop. Such analyses are obtained by means of extremely accurate FEM simulations by varying the boundary conditions on the cooling surfaces and evaluating the self- and mutual- heating thermal resistances of the devices; the DSC modules demonstrated to be a good choice only if a good boundary condition is granted (i.e., when a good cooling system is available) with a reduction up to 40% on the thermal resistance.

A study of the breakdown voltages of DSC modules has been conducted; it demonstrated a result that goes in an opposite way to the expected outcome. A typical choice to improve the electrical ruggedness of DSC modules consists in a high spacing between the two substrates composing it; in this way, the capacitive effects are apparently reduced. We discovered that, by reducing the spacing in between the substrates, the breakdown voltage increases. First, simulations were exploited to evaluate and provide an explanation to this effect, then many experiments were conducted to confirm our study. These analyses allowed to produce a conference paper in the ISAPP 2019 symposium, which has been presented by be in Osaka (Japan). I am currently working to extend this paper on a Journal.

GaN-based circuits on PCB – GaN technology represents an opportunity in power electronics to achieve very high switching frequency, thus enabling higher volumetric and gravimetric power density, strategic to the competitive development of many application domains as hybrid and electric transport. Since GaN-based circuits are still mainly realized using discrete components on PCB, their thermal management can be critical because the difficulties in containing the number of interfaces between the devices and the cooling environment. The choice of cooling solutions for the circuits on PCB is usually supported by numerical simulations or experimental characterizations, both requiring time and technical skills; to alleviate the work of the thermal designers, I developed simple analytical models to predict the impact of cooling solutions like thermal vias and heat-sinks; such

MOR approach – FEM thermal simulations are usually expensive in terms of time. The model-order reduction approach developed by prof. Lorenzo Codecasa allows to perform thermal simulations with a given value of error in relatively short time. I took part of its work by providing a simulation example based on GaAs multi-emitter HBTs.

Collaboration:

Politecnico di Milano – Prof. Lorenzo Codecasa

Qorvo inc. – Peter J. Zampardi, Brian Moser

University of Nottingham – Prof. Alberto Castellazzi, Dr. Asad Fayyaz

Primes Innovations Laboratories– Dr. Philippe Laserre, Dr. Cyrille Duchesne

#### 4. Products

##### a. Publications as Journal papers

- I. L. Codecasa, **A. P. Catalano**, and V. d'Alessandro, "A-priori error bound for moment matching approximants of thermal models," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2019.

##### b. Publications as Conference papers

- II. R. Trani, **A. P. Catalano**, A. Castellazzi, and V. d'Alessandro, "Thermal management solutions for a lightweight 3L GaN inverter," *Proc. ICPE - ECCE Asia*, 2019.

- III. **A. P. Catalano**, V. d'Alessandro, P. Guerriero, and S. Daliento, "Diagnosis of power losses in PV plants by means of UAV thermography," *Proc. IEEE International Conference on Clean Electrical Power*, pp. 306–310, Jul. 2019.
- IV. **A. P. Catalano**, C. Scognamillo, A. Castellazzi, and V. d'Alessandro, "Optimum thermal design of high-voltage double-sided cooled multi-chip SiC power modules," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- V. **A. P. Catalano**, R. Trani, A. Castellazzi, and V. d'Alessandro, "Analytical modeling of through-PCB thermal vias and heat-sinks for integrated power electronics," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- VI. **A. P. Catalano**, V. d'Alessandro, P. Guerriero, and S. Daliento, "Diagnosis of power losses in PV plants by means of UAV thermography," *Proc. IEEE International Conference on Clean Electrical Power*, pp. 306–310, Jul. 2019.
- VII. **A. P. Catalano**, C. Scognamillo, A. Castellazzi, and V. d'Alessandro, "Optimum thermal design of high-voltage double-sided cooled multi-chip SiC power modules," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- VIII. **A. P. Catalano**, R. Trani, A. Castellazzi, and V. d'Alessandro, "Analytical modeling of through-PCB thermal vias and heat-sinks for integrated power electronics," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- IX. P. Guerriero, **A. P. Catalano**, I. Maticena, L. Codecasa, V. d'Alessandro, and S. Daliento, "Experimental assessment of malfunction events in photovoltaic modules from IR thermal maps" *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- X. C. Scognamillo, **A. P. Catalano**, R. Trani, V. d'Alessandro, and A. Castellazzi, "Influence of bumps height on electric field in double sided cooling power modules," *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.
- XI. R. Trani, **A. P. Catalano**, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Optimum thermal management design for compact PCB-based high frequency GaN assemblies" *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.
- XII. **A. P. Catalano**, O. Olanrewaju, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Stress-induced vertical deformations in state-of-the-art power modules: an improved electro-thermo-mechanical approach," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).
- XIII. C. Scognamillo, **A. P. Catalano**, R. Trani, V. d'Alessandro, and A. Castellazzi, "Influence of bumps height on electric field in double sided cooling power modules," *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.
- XIV. **A. P. Catalano**, R. Trani, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Optimization of thermal vias design in PCB-based power circuits," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).

*Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).

- XV. C. Scognamillo, **A. P. Catalano**, R. Trani, V. d'Alessandro, and A. Castellazzi, "3-D FEM investigation on electrical ruggedness of double-sided cooling power modules," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).

## 5. Conferences and Seminars

IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 25-27 Sep. 2019, Lecco (Italy).

International Symposium on Advanced Power Packaging (ISAPP), 7-8Oct. 2019, Osaka (Japan).

## 6. Activity abroad

From February to July I visited 'University of Nottingham' in UK. There, I studied thermal and electrothermal problems in power devices, circuits, and systems; prof. Alberto Castellazzi was my tutor. During my abroad period, I published 7 conference papers on such topics.

## 7. Tutorship

- Master of Science correlator: The students Ciro Scognamillo and Roberto Trani have been supported by me for their MSc thesis. I spent **40 hours** to introduce them the instruments and the methodologies to carry out results for their thesis. They reached me in University of Nottingham from April to July 2019 and graduated in October 2019.
- Bachelor of Science correlator: The student Maria Diletta Pavone have been supported by me for her BSc thesis. I spent **20 hours** showing her the approaches to perform electrothermal simulations in PSPICE OrCAD. She graduated in December 2019-
- Assistant for the BSc course "Elettronica Digitale", held by Prof. Vincenzo d'Alessandro, **5 hours**.