PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Antonio Pio Catalano

XXXII Cycle

Training and Research Activities Report – First Year

Tutor: Prof. Vincenzo d'Alessandro

1. Information

I received the M. Sc. Degree, cum laude, in Electronic Engineering from University of Napoli 'Federico II' in October 27th 2016 with the thesis "*Numerical Optimization of GaAs HBT Thermal Ruggedness with Design Of Experiments".* I belong to XXXII cycle of Information Technology and Electrical Engineering (ITEE) PhD. My fellowship is financed by athenaeum. My tutor is Prof. Vincenzo d'Alessandro.

2. Study and Training activities

During this first year I followed courses to improve my knowledge in (i) Radio Frequency circuits and their applications and (ii) digital electronics. I attended a lot of seminars to extend my culture in other topics of Information Technology.

Study and training activities are summarized below:

a. Modules

- RF bootcamp – Prof. Marco Spirito
- Satellite Remote Sensing: open challenges and opportunities – Prof. Giuseppe Ruello
- System on Chip – Prof. Nicola Petra

b. Seminars

- Electromechanical Consequences of violent instabilities in Tokamaks – Prof. Pustovitov
- IBM Cognitive Computing – Dott. Leo
- Cognitive Computing and Da Vinci Robot – Prof. Maresca
- Presentazione Aziendale: "Infineon Technologies" – Ing. Cristiano
- Superconduttività: opportunità di sviluppo e di trasferimento tecnologico – Prof. Salatino
- Wide-Band-Gap Semiconductor Based Electrical Power Conversion – Prof. Castellazzi
- (Effective) Machine Learning in the Time of Big Data – Prof. Corazza
- SeeQC-eu, Hypres Quantum Engineering Company in Europe - Dott. Mukhanov

c. External courses

During the 1st year I didn't attend external courses.

	Credits year 1							
		1	2	3	4	5	6	
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary
Modules	20	3	0	0	0	3	9	15
Seminars	5	1,9	0	0	3	0,8	0,3	6
Research	35	5,1	10	10	5	5,2	3,7	39
	60	10	10	10	8	9	13	60

3. Research activity

My research activity is about high-accurate thermal simulations of electronic devices. The analyzed devices take part of two different groups: (i) Gallium Arsenide based Heterojunction Bipolar Transistors (HBTs) for radio frequency (RF) applications and (ii) VDMOS and IBGTs for power applications. The same simulation approach and tools have been used for both, but the results obtained are different. This section has been divided in two topics as follows:

GaAs-based HBT for RF applications - The GaAs technology is widely used to develop high performance devices in every field of electronic. Heterojunction Bipolar Transistors (HBTs) are the dominant technology for handset power amplifier design by virtue of features like high power density, cut-off frequency, and efficiency [1]. Unfortunately, these devices are plagued by electrothermal effects due to mesa isolation and low thermal conductivity of GaAs (one third of that of silicon), which - combined with high operating currents - can lead to performance degradation, long-term reliability issues, and also sudden device failure (as an example, biased with a constant base current may suffer from performance-limiting or even destructive current gain collapse [2]). My research activity is in this scenario.

My first research work has been done starting from the MSc thesis; it concerns single-Mesa (with only one Unit Cell) devices and is focused on the evaluation of thermal performances in terms of thermal resistance (Rth). Since the early eighties, the literature is populated by papers centered on the impact of metallization layers on the thermal resistances [3] with their shunt and spread effects useful for drain off heat; little attention was instead paid to other technology features like the specifics of the emitter stack (with the exception of [4]). For this work, published as conference paper [II], models for thermal resistances of devices with different emitter size have been built; these models describe Rth as functions of technology parameters (thicknesses of semiconductor and metal layers) of interest. The models are based on the *Design Of Experiment* procedure; for each model, has been needed about 30 FEM high-accurate purely-thermal simulations in addiction to about 70 more to verify the models goodness. In order to obtain this huge number of simulation, an automatic tool has been developed which allows to obtain extensive session of analyses starting from automatic generation of 3D geometry and meshing, and, subsequently, simulating the thermal FEM problem.

In literature has been investigated the beneficial effect of a more thermally conductive and/or shorter path from the heat dissipation region and the sink, which can be obtained with flip-chip packaging [5], or alternative solutions based on thermal vias [6]. Starting from these topics, another research activity of mine has concerned the analyses of packaging techniques; the (more common) wire-bonding and flip-chip features, including the effect of laminate, have been compared in terms of thermal performance. This work has led us to publish a conference and a journal paper, respectively [III] and [I]. Also in this case, an automatic tool for purely thermal simulations has been used; it has been developed starting from the skills obtained during previous work.

My last research activity about this area is about the extraction of Thermal Feedback Block (TFB) for steady-state electrothermal analyses of multi-Mesa (with more than two Unit Cells) HBTs. This will be the main topic for my future research activity. My target, currently, is to investigate the electrothermal effects of bipolar devices thanks our ultra-fast and accurate ET analyses. The developed tools for these simulations had led to a conference paper [VI], to be presented at April 2018.

Si-based IGBT and SiC-based VDMOS for power applications - Devices, circuit and systems for power applications are characterized by high operating temperature due to the large dissipated power. The temperature increase entails electrothermal effects that reduce their performance, reliability, and lifetime [7]. From a thorough industry survey, it was found that active devices are the most fragile

components in most applications [8]. As a consequence, ET simulations coupling the thermal and electrical problems are needed to perform a thermal-aware design. These analyses can be conducted both on cell-level [9] and on module-level [10].

My research activity in this area has been centered on (i) cell-level ET device simulation of SiC-based VDMOS and (ii) module-level ET circuit simulation (buck converter) using Si-based IGBT power module; these analyses had led to publish 2 conference papers, respectively [V] and [IV]. My role for these publications has been to build the TFB netlists starting from dynamic purely-thermal simulations. During my future research activity about this topic, I want to study the procedures of parameters extraction for the electrical model of power devices.

References:

[1] M. Fresina, “Trends in GaAs HBTs for wireless and RF,” in *Proc. IEEE BCTM*, 2011.
[2] W. Liu *et al.*, “Current gain collapse in microwave multifinger heterojunction bipolar transistors operated at very high power densities,” *IEEE Transactions on Electron Devices*, vol. 40, no. 11, pp. 1917–1927, Nov. 1993.
[3] L. L. Liou, B. Bayraktaroglu, C. I. Huang, and J. Barrette, “The effect of thermal shunt on the current instability of multiple emitter-finger heterojunction bipolar transistors,” in *Proc. IEEE BCTM*, 1993, pp. 253–256.
[4] R. Anholt, “HBT thermal element design using an electro/thermal simulator,” *Solid-State Electronics*, vol. 42, no. 5, pp. 857–864, May 1998.
[5] J. Aiden Higgins, “Thermal properties of power HBT’s,” *IEEE Transactions on Electron Devices*, vol. 40, no. 12, pp. 2171–2177, Dec. 1993.
[6] D. Hill *et al.*, “Novel HBT with reduced thermal impedance,” *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 11, pp. 373–375, Nov. 1995.
[7] G. Breglio *et al.*, “Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching,” *IEEE Trans. Electron. Devices*, vol. 60, no. 2, pp. 563–570, Feb. 2013.
[8] S. Yang *et al.*, “An industry-based survey of reliability in power electronic converters,” *IEEE Trans. Industry Applications*, vol. 47, no. 3, pp. 1441–1451, Mar. 2011.
[9] V. d’Alessandro *et al.*, “SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs,” *Proc. IEEE ISPSD*, 2014, pp. 285–288.
[10] S. Yang *et al.*, “An industry-based survey of reliability in power electronic converters,” *IEEE Trans. Industry Applications*, vol. 47, no. 3, pp. 1441–1451, Mar. 2011.

Collaborations:

Politecnico di Milano – Prof. Lorenzo Codecasa

Qorvo inc. – Peter J. Zampardi, Brian Moser

4. Products

a. Publications as Journal papers

I. V. d'Alessandro *et al.*, "Simulation comparison of InGaP/GaAs HBT thermal performance in wire-bonding and flip-chip technologies," *Microelectronics Reliability*, vol. 78, pp. 233-242, 2017.

b. Publications as Conference papers

II. A. P. Catalano *et al.*, "Influence of layout and technology parameters on the thermal behavior of InGaP/GaAs HBTs," *Ph. D. Research in Microelectronics and Electronics (PRIME), 2017 13th Conference on.* IEEE, 2017.

III. A. P. Catalano *et al.*, "Numerical analysis of the thermal behavior sensitivity to technology parameters and operating conditions in InGaP/GaAs HBTs," *Compound Semiconductor Integrated Circuit Symposium (CSICS).* IEEE, 2017.

IV. A. P. Catalano *et al.*, "Model-Order Reduction Procedure for Fast Dynamic Electrothermal Simulation of Power Converters," *Applications in Electronics Pervading Industry, Environment and Society: (APPLEPIES), 2017* Springer, 2017.

V. A. P. Catalano *et al.*, "Effect of heat source modeling in DC circuit-level electrothermal simulation of power MOSFETs," *proceedings of 49th SIE conference,* 2017.

VI. V. d'Alessandro *et al.*, "Combined SPICE-FEM Analysis of Electrothermal Effects in InGaP/GaAs HBT Arrays for Handset Applications," *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2018 19th International Conference on.* IEEE, 2018. (accepted as Keynote presentation)

5. Conferences and Seminars

IEEE Ph.D. Research in Microelectronics and Electronics (PRIME) conference - Giardini Naxos (ME), Italy – June 2017 – Paper presented by me as oral

Applications in Electronics Pervading Industry, Environment and Society (APPLEPIES) conference – Roma (RM), Italy – September 2017 – Paper presented by me as oral

6. Activity abroad

During my 1st PhD year I didn’t spend time aboard.

7. Tutorship

- Bachelor of Science correlator: The student Ciro Scognamillo has been supported by me for his BSc thesis. I spent **30 hours** to introduce the main topics and software for his work. Ciro Scognamillo graduated in Electronic Engineering at day October 23th 2017, magna cum laude, with prof. d’Alessandro as relator discussing the thesis “*Development of routines for the automated generation and solution of 3-D FEM thermal models of InGaP/GaAs bipolar transistors for power amplifiers* “.

- Assistant for the BSc course “Elettronica Digitale” and MSc course “Microelettronica”, held by Prof. Vincenzo d’Alessandro, **10 hours.**