PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Gerardo Castellano

XXX Cycle

Training and Research Activities Report – Second Year

Tutor: Davide De Caro

1. Information

I received the M.S. degree cum laude in Electronic Engineering the 26th March 2014 from University of Napoli "Federico II". From June to October 2014 I received a scholarship as part of the research project "VEM, Virtual Energy Management". I belong to XXX cycle of ITEE PhD and Marvell (Italia) - DIETI finance my fellowship in VLSI systems. My tutor is Prof. Davide De Caro.

2. Study and training activities

Module	Type	CFU
IEEE Circuits and Systems (CAS) Day – Como 2016	Doctoral School	1
Topics on Microelectronics – Pavia 2016	Doctoral School	4
Rohde & Schwarz Research & Education Seminar Tour 2016 "New Frontiers in RF Measurements" – Pavia 2016	Doctoral School	1

Seminar	Date	CFU
Memory technologies for Android based systems	10/11/2015	0.4
Test and Diagnosis of Integrated Circuits	17-18/11/2015	2.4
Hardware Security and Trust	19-20/11/2015	2.4
Gallium Nitride for power applications: benefits, challenges, and state of the art	16/12/2015	0.4

	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0	3	0	7	1	5	**16**	14	0	0	1	5	0	0	**6**	8							**0**	**22**	30-70
Seminars	5	0	0,6	2,2	1,4	0	0,2	**4,4**	5	5,6	0	0	0	0	0	**5,6**	0							**0**	**10**	10-30
Research	35	10	6	8	2	9	5	**40**	41	5	10	9	5	10	10	**49**	52							**0**	**89**	80-140
	60	10	9,6	10	10	10	10	**60**	60	11	10	10	10	10	10	**61**	60	0	0	0	0	0	0	**0**	**121**	180

3. Research activity

The main theme of my research activity is VLSI Digital systems; in particular, in this second year, I have focused the design and testing of SAW-less digitally-assisted receivers for next generation of wireless mobile terminals. In the last years special emphasis has been dedicated to hand-held wireless terminals, which continue to evolve from simple phones to ever more complicated and versatile smart computing machines. The exponentially increasing complexity of such smartphone is due to the ever growing demand of performance, standard, modes of operations and bands to be supported. For each band, dedicated narrowband off-chip SAW filters are used to eliminate large out-of-band blockers. Solutions that make possible to replace off-chip filters with equivalent integrable circuits, allowing to reduce system cost, complexity and area, are highly desirable.

a) **Hybrid transformer-based receiver** *(completed research activity)*

In frequency division duplex (FDD) applications, in which transmitter (Tx) and receiver (Rx) share the same antenna, SAW-based duplexers are used to provide sufficient Tx-Rx isolation. In this scenario, the hybrid transformer has been recently proposed [1]-[3] to replace multiple off-chip duplexers with a single reconfigurable solution; however, in a hybrid-based duplexers, the issue is the sensitivity of the Tx–Rx isolation to the antenna impedance. In fact, the isolation level is a function of the matching between the antenna impedance (e.g. a common planar F-inverted antenna used in modern mobile phone) and a suitably designed balancing impedance. The antenna impedance is strongly frequency dependent and it changes with time due to interactions with the external environment. Therefore, antenna impedance variability must be dealt with in frequency by ensuring isolation across the desired bandwidth and in time domain by adaptively adjusting the balancing impedance to track the antenna impedance variations. The idea behind this work is to provide a system analysis and to demonstrate a hardware implementation of a mixed-signal low power control system, tailored to an integrated duplexer receiver prototype compatible with the 3G standard [1] and able to ensure a real-time control of the Tx-Rx isolation level. The complete tested system includes the hybrid transformer-based receiver [1], the digital control system implemented on a FPGA and two analog-to-digital converters (ADCs) at the interface. The digital control, through real-time baseband measurements of the Tx leakage power in the Rx path, is able to find the optimum balancing impedance value which maximizes the Tx-Rx isolation (*optimization phase*) and to track the variations during the normal functioning of the system (*tracking phase*). Considering as main goal the low-power low-area hardware implementation of the control system, a simple customized gradient descent method was developed to solve the optimization problem. Moreover, to further simplify the algorithm implementation and increase its noise immunity, only the sign of the gradient is effectively measured to identify the right direction toward which move the programmable balancing impedance, controlling it like in the binary search method. This optimization phase is normally carried out only at start-up or after a major change in the operating conditions, whereupon the control system switches in the tracking phase to keep the Tx-Rx isolation high at all times. The interactions between the antenna and the external environment lead to a slow drift of the optimal point that the control network must be able to track in real-time. Since the variations of the optimum point are inherently much slower with respect to the settling time of the control system, only a few LSBs need to be adjusted in order to follow the antenna impedance variations. Briefly, the tracking phase works similarly to the previous one, but exploiting a step size of a single LSB on the control the balancing impedance variables to avoid sudden drop in the Tx-Rx isolation. Both the optimization and tracking phase exploit the information provided by the gradient components to find the optimum point. These components are estimated through real-time Tx leakage measurements, that are corrupted by noise. The error probability to get a wrong estimation of the gradient components sign depends on the input signal to noise ratio (SNR): the higher is the SNR, the higher is the error probability. However, the SNR can be easily improved in

digital domain to verify the maximum tolerated error probability, taking multiple measurements of the signal of interest and estimating its mean value, obviously resulting in a convergence times worsening. The presented approach belongs to the general class of the so-called Monte Carlo methods: the control system, according to the input SNR, adaptively defines the measurement time to verify the maximum tolerated error probability but, the lower is the input SNR, the higher is the convergence time of the control system. Therefore, considering that several works prove that relevant variations in the antenna impedance occur on a time scale of a few milliseconds (e.g. >10 ms in [4]), the optimization process should be performed in a sufficiently small time (e.g. <100 μs) to ensure static conditions. For the designed control network, to perform all the optimization process in less than 100μs, ensuring an error probability of 0.1%, the required SNR_{min} > -5 dB. Even if, in our experiments, the main receiver was tuned to the Tx carrier frequency and used to validate the control system, in a real FDD application an auxiliary receiver with much relaxed performances, and hence very low power, should be added in parallel to the main one only to sense the Tx leakage for the digital control network without interfering with the normal operation of the main transceiver. We have demonstrated that the required sensitivity, 1-dB compression point and NF of the auxiliary receiver should be, respectively, P_{sens} < -91 dBm, P_{1dB} > -26 dBm and NF < 21dB. As an example, the receiver in [4] meets these requirements with only 0.6mW of power. Concluding, the performance of the proposed control system has been experimentally verified using the main receiver [1] as RF front-end, a Cyclone IV Altera FPGA to synthesize the digital control and two configurable ADCs placed at the end of the down-conversion chain. In this setup configuration, SNR_{min} = 6dB, limited only by the ADCs resolution, and hence the worst case convergence time of the optimization algorithm should be ≈100μs but, thanks to the Monte Carlo approach, faster convergence is normally expected. The experimental results confirm the above prediction, demonstrating that the optimization process is completed in ≈80μs and the tracking phase keeps a high isolation level even with work environment changing.

[1] M. Ramella, I. Fabiano, D. Manstretta, and R. Castello, “A 1.7-2.1GHz +23dBm TX Power Compatible Blocker Tolerant FDD Receiver with Integrated Duplexer in 28nm CMOS”, Proc. of IEEE ASSCC, Nov 2015
[2] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, “Tunable CMOS Integrated Duplexer with Antenna Impedance Tracking and High Isolation in the Transmit and Receive Bands”, IEEE Trans. on MTT, pp. 2092–2104, Sep 2014.
[3] B. Hershberg, B. van Liempd, X. Zhang, P. Wambacq, J. Craninckx, “A Dual-Frequency 0.7-to-1GHz Balance Network for Electrical Balance Duplexers”, Proc. of IEEE ISSCC, pp 356-358, 2016.
[4] A. Selvakumar, M. Zargham and A. Liscidini, “Sub-mW Current Re-Use Receiver Front-End for Wireless Sensor Network Applications”, in IEEE JSSC, vol. 50, no. 12, pp. 2965-2974, Dec. 2015.

b) **SAW-less diversity receiver** *(ongoing and future research activity)*

A typical mobile communication system is made of a main transceiver and one or more diversity receivers (*MIMO* structure). This approach is a way to add redundancy to the reception of the signal, improving the capacity and the quality of the communication channel. Usually the main receiver and the transmitter share the same antenna through a SAW-based duplexer, while the diversity receiver has a dedicated antenna. This scenario is particularly critical in a FDD system: due to the proximity of the two antennas, part of the transmitted signal can be coupled to the diversity receiver. The poor linearity of the diversity receiver, the reciprocal mixing of the TX leakage with the phase noise of the local oscillator and the transmitter broadband noise that directly falls into the receiver band could bring the receiver to desensitization. To avoid these drawback, an off-chip SAW filter is commonly used to filter out the self-interference component as well as unwanted out-of-band interferers coming from the external environment. That we propose to solve all these problems in a SAW-less diversity receiver is a complex mixed-signal system fully integrated. At the input of the diversity receiver the small wanted signal comes with out of band blocker and the strong transmitter leakage signal. Therefore, a main canceler is used to reduce the TX leakage power at the beginning of the receiving chain, relaxing the linearity requirement of the chain. However, since the blocker is still there, we need a highly linear receiver yet. The last step is the reduction of the TX noise that falls into the RX band: an auxiliary

receiving chain provides a digital-domain copy of the TX noise in the RX band, allowing to the digital equalizer to filter out the noise from the desired weak signal, relaxing the receiver noise requirements.

4. Products

a. Journal papers
   I. E. Napoli, G. Castellano, D. De Caro, D. Esposito, N. Petra, A.G.M. Strollo, "A SISO register circuit tailored for input data with low transition probability", IEEE Transaction On Computers (early access), 2016.
   II. D. De Caro, F. Tessitore, G. Vai, G. Castellano, E. Napoli, N. Petra, C. Parrella, A. G. M. Strollo, "Single flip-flop driving circuit for glitch-free NAND-based digitally controlled delay-lines", Springer Circuits and Systems for Signal Processing, 2016.
   III. G. Castellano, D. Esposito, P. Bifulco, D. De Caro, E. Napoli, N. Petra, M. Cesarelli, A.G.M. Strollo, "A Real-Time Spatio-Temporal IIR Filter for Poisson Video Denoising with Application to X-ray Fluoroscopy", IEEE Transaction On Circuits and Systems for Video Technology, submitted.

b. Conference papers
   I. G. Castellano, D. De Caro, A. G. M. Strollo, D. Manstretta, "A Low Power Control System for Real-Time Tuning of a Hybrid Transformer-based Receiver", 2016 IEEE International Conference on Electronics Circuits and Systems (to be presented).
   II. E. Napoli, G. Castellano, D. Esposito, A.G.M. Strollo, "Digital Circuit for the Generation of Colored Noise Exploiting Single Bit Pseudo Random Sequence", 2016 7th IEEE Latin American Symposium on Circuits and Systems, pp. 23-26, 2016.
   III. D. Esposito, G. Castellano, D. De Caro, E. Napoli, N. Petra, A.G.M. Strollo," Approximate Adder With Output Correction for Error Tolerant Applications and Gaussian Distribuited Inputs", 2016 IEEE International Symposium on Circuits and Systems, pp. 1970-1973, 2016.

5. Conferences and Seminars

No Conference or Seminar has been kept in this year.

6. Activity abroad

No activity abroad has been carried out in this year.

7. Tutorship

Correlator of M.S. thesis "Sviluppo di un circuito per il filtraggio in Real-Time di video fluoroscopici", Student: Antonio Angelino - 20 hours.