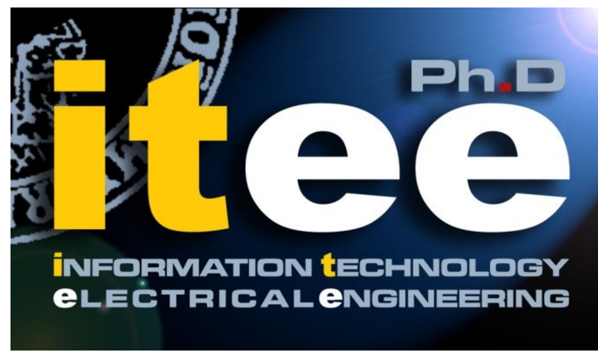


Alessandro Borghese

Tutor: Prof. Andrea Irace

XXXIV Cycle - III year presentation

Study of Wide Bandgap Devices

Background

Alessandro Borghese received his BSc and MSc degrees in **electronic engineering** from the University of Naples Federico II.

-Master thesis (Oct. 23rd, 2017)

"Efficiency Estimation and Comparison of Two Inverters for Electric Vehicles: Si vs. SiC Power Devices". Technical Centre of **Toyota** Motor Europe (Belgium).

Nov. 2017 - Oct. 2018

Worked at **Electrothermal Characterization Laboratory** (DIETI, University of Naples Federico II).

Oct. 2018,

Public admission procedure **34th cycle ITEE PhD**. Awarded w/ a **grant from Ateneo Federico II**

tutor: **Prof. Andrea Irace**.

My research activity is focused on power electronics, specifically on wide bandgap power semiconductor devices.

power semiconductor devices

Think of them as switches

1. **Allow any current flow when closed**
2. **Block any voltage when open**
3. **Instantaneous commutations**

wide bandgap power semiconductor devices are semiconductors more suited to this task

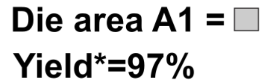
The most technologically ready are

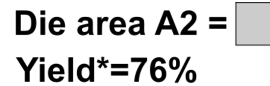
Silicon Carbide **SiC**

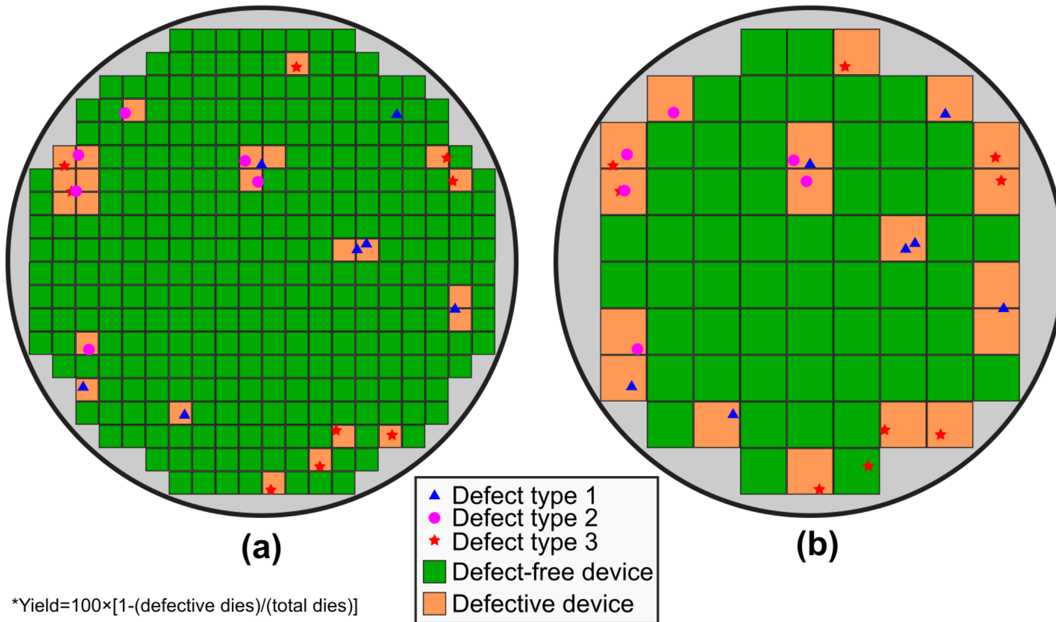
Gallium Nitride **GaN**

Effect of Parameters Spread on the performance of SiC Power Modules

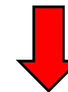
SiC MOSFET – current rating limitation







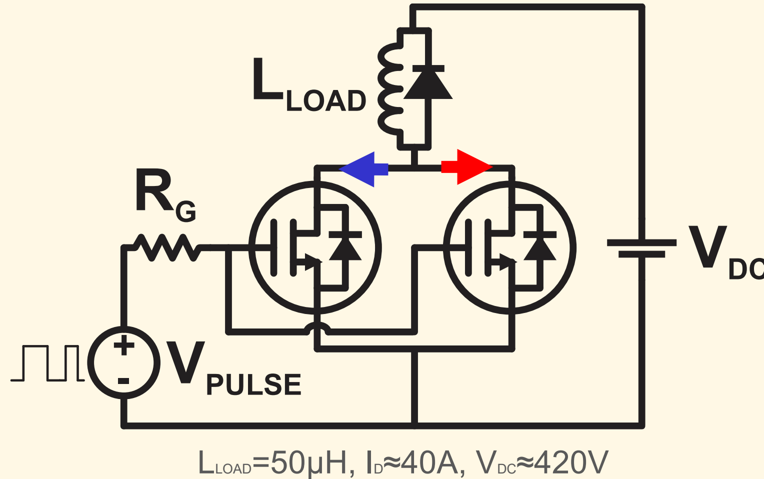
- **SiC MOSFETs**
  - enable **more efficient** and **compact converters** thanks to excellent static and dynamic performances
  - **not available at high current levels (>200A)**



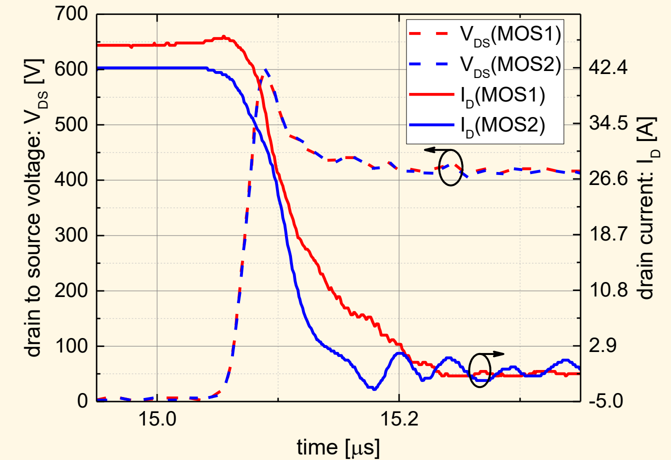
↗die size = ↘yield ➔ Great interest in **multichip (parallel) structures (Power modules)**

Electrothermal imbalances in parallel SiC MOSFETs

Inductive turn-off of **2 parallel SiC MOSFETs**



L_{LOAD}=50µH, I_D≈40A, V_{DC}≈420V

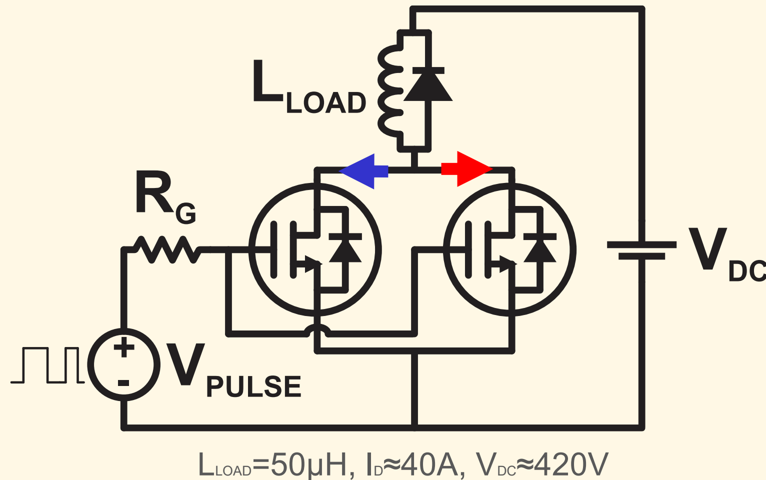


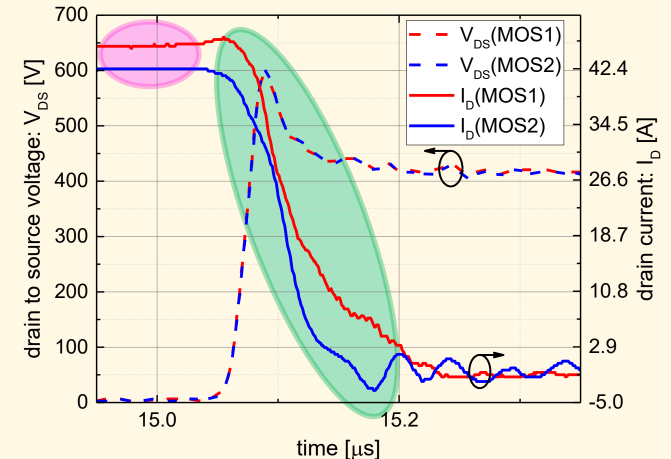
Device & circuit parameters mismatches → Unbalanced devices behavior → Uneven temperature rise → Shorter lifetime

Derating rules & design optimization needed to reliably parallel SiC MOSFETs

Sources of current imbalance

Inductive turn-off of **2 parallel SiC MOSFETs**





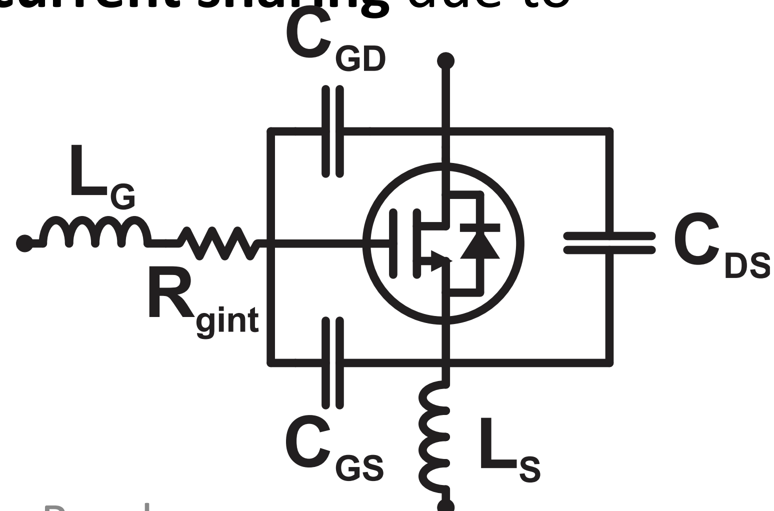
Static and transient **unbalanced current sharing** due to Mismatched

-**Device** parameters:

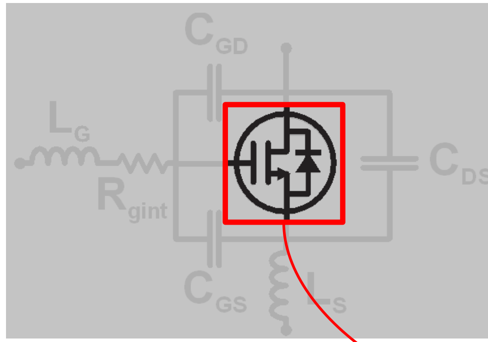
V_{TH}, R_{ON}, C_{DS}, C_{GD}, C_{GS}

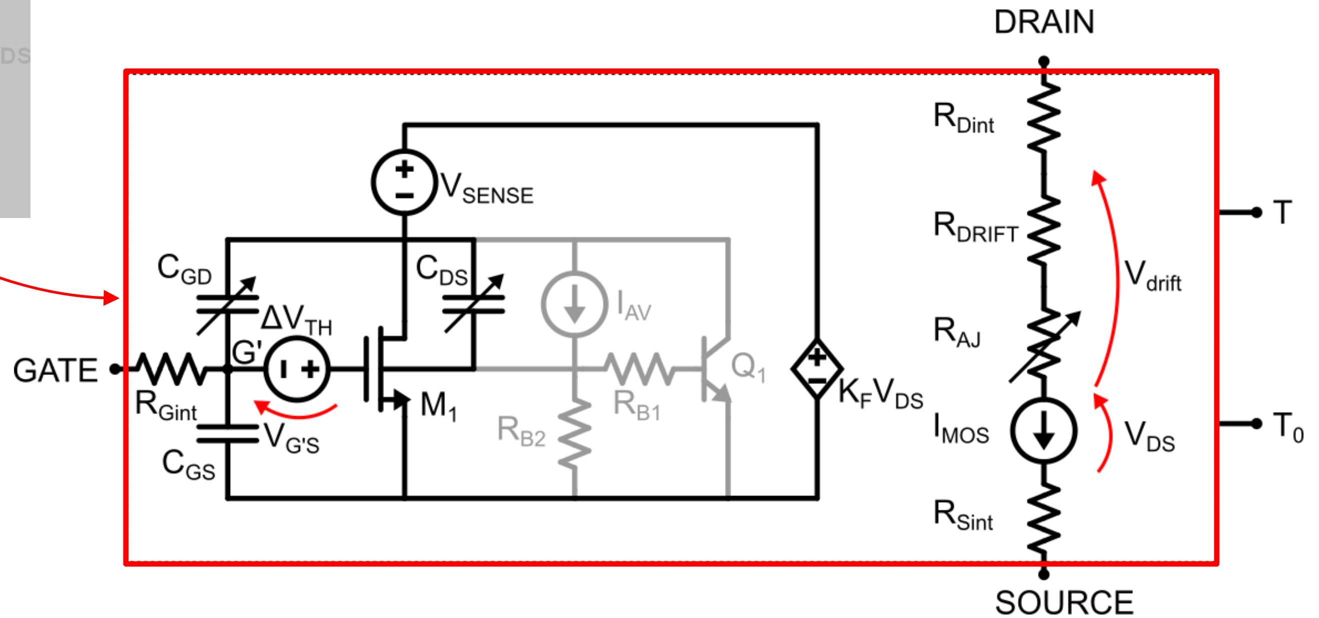
-**Circuit** parameters

L_S, R_{gint}, L_G



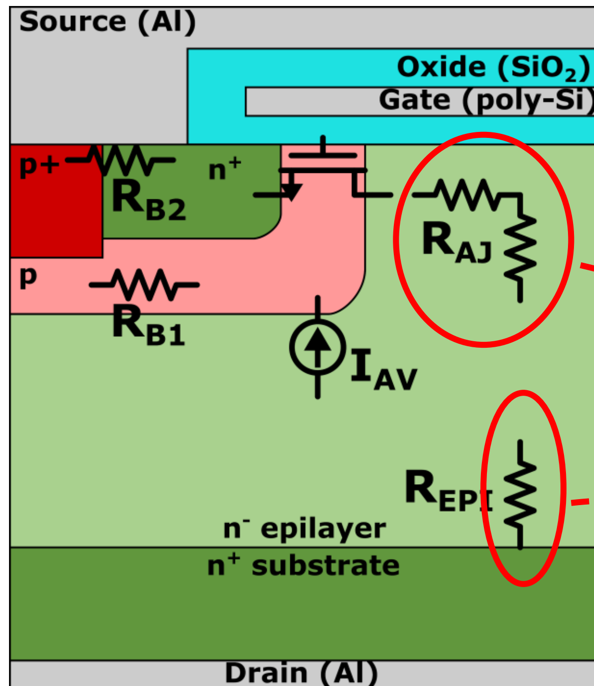
Model subcircuit





Model subcircuit – derivation

The model is derived from the one used for Silicon VD MOSFET: the **most crucial part** is demanded to the **non-linear drain resistance**.



$$R_D\left(V_{GS},V_{drift},T\right)=R_{AJ}\left(V_{GS},V_{drift},T\right)+R_{EPI}\left(T\right)$$

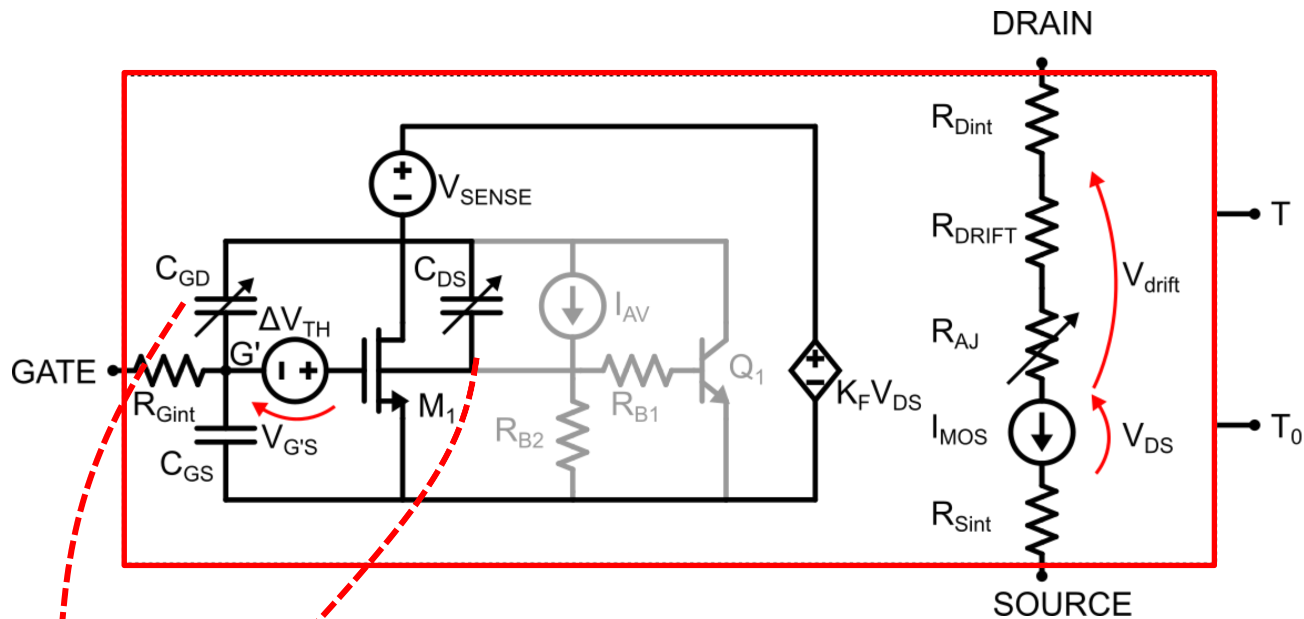
$$R_{AJ}\left(V_{GS},V_{drift},T\right)=\frac{V_{drift}}{V_1+V_{drift}}\cdot\left[R_{AJ1}\left(T\right)+R_{AJ2}\left(T\right)\left(1+\frac{V_{GS}}{V_2}\right)^{-\eta}\right]$$

$$R_{EPI}\left(T\right)=R_{EPI0}\left(\frac{T}{T_0}\right)^{r_0}$$

Temperature dependence of the 'bulk' electron mobility even for T>500 K*

$$\mu_L\left(T\right)=\mu_{L0}\left(\frac{T}{300}\right)^{-r+\alpha T/300}$$

Model subcircuit - capacitances



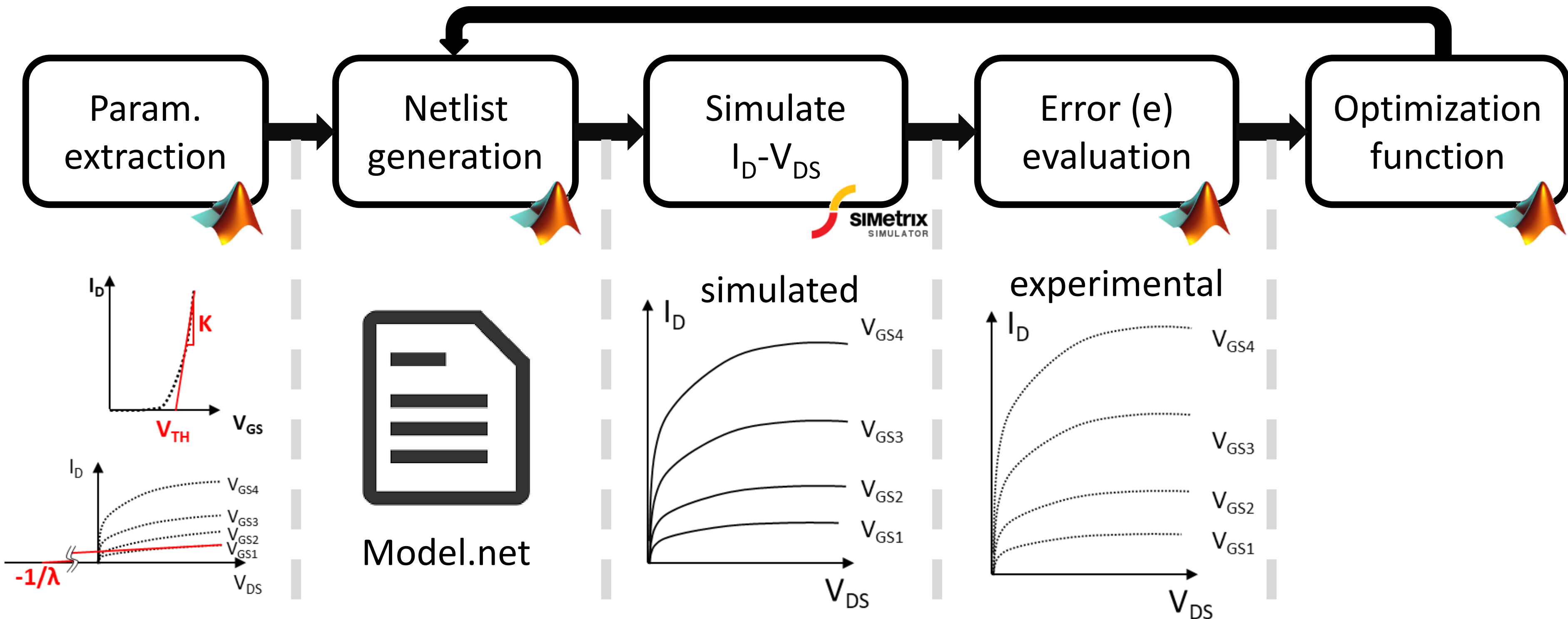
$$C_{DS}(V_{ds}) = \frac{C_{DS0}\left[\frac{\pi}{2} + \arctan\left(-\frac{V_{ds}}{V_{ds}^{*}}\right)\right]}{\pi/2} + C_{DSMIN}$$

$$C_{GD}(V_{gd}) = (C_{GD0} - C_{GDMIN})\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_{gd}}{V_{gd}^{*}}\right)\right] + C_{GDMIN}.$$

Model calibration

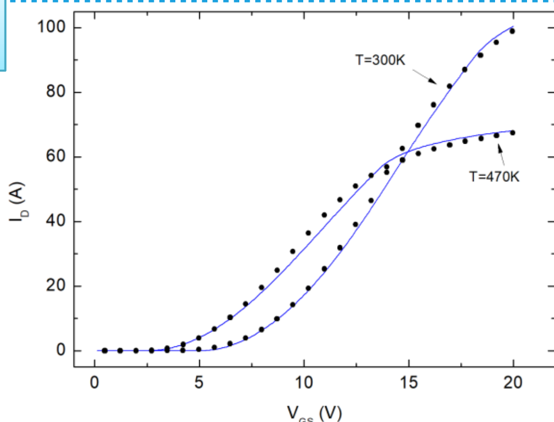
The **complete model** with all the temperature dependences is **based on 38 parameters**, some of which have a physical meaning and can be directly extracted from measured data.

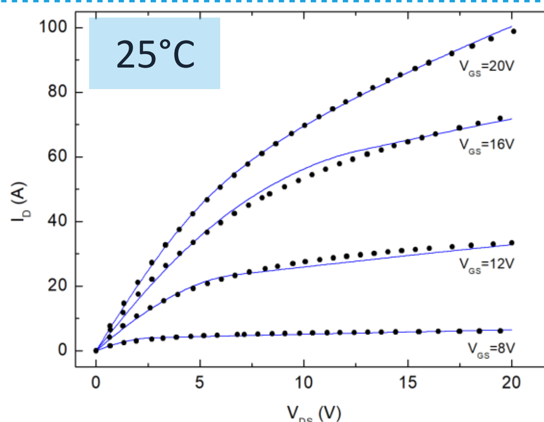
Calibration=tuning the model parameters so that it matches experimental electrical waveforms

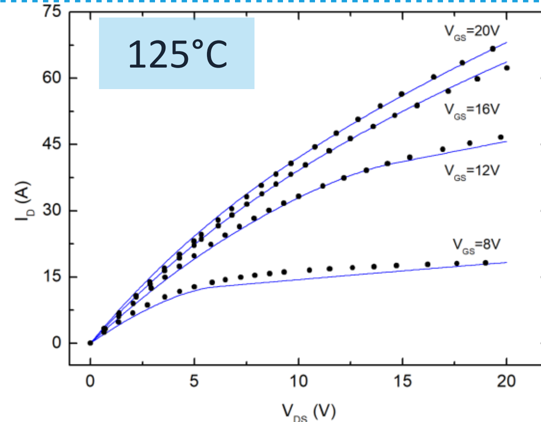


Model Validation – 1.2 kV device

DC

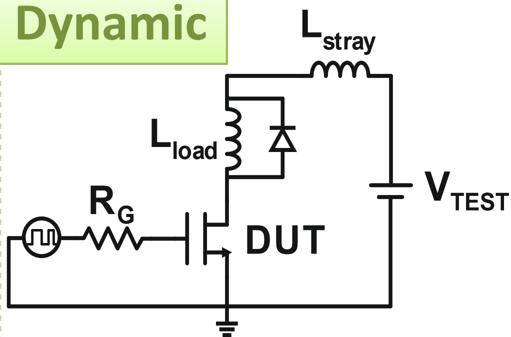


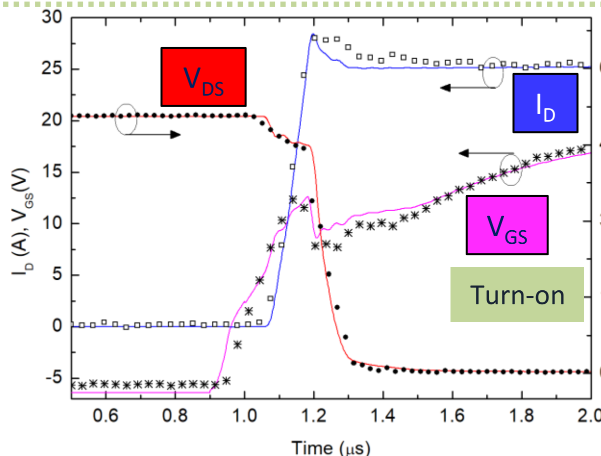


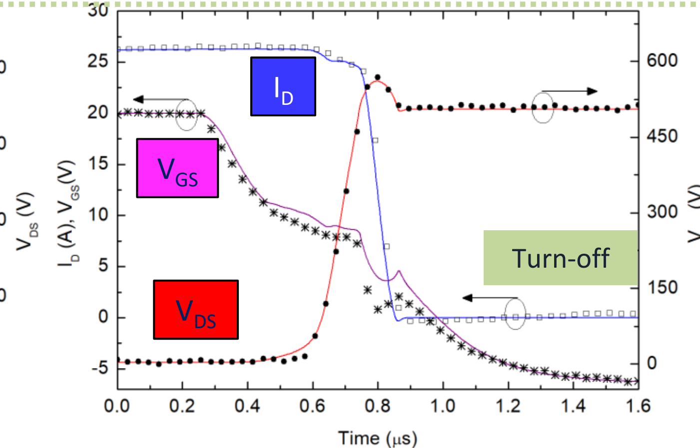


Good prediction for a wide range of V_{GS}, including the soft transition between linear and saturation regs.

Dynamic





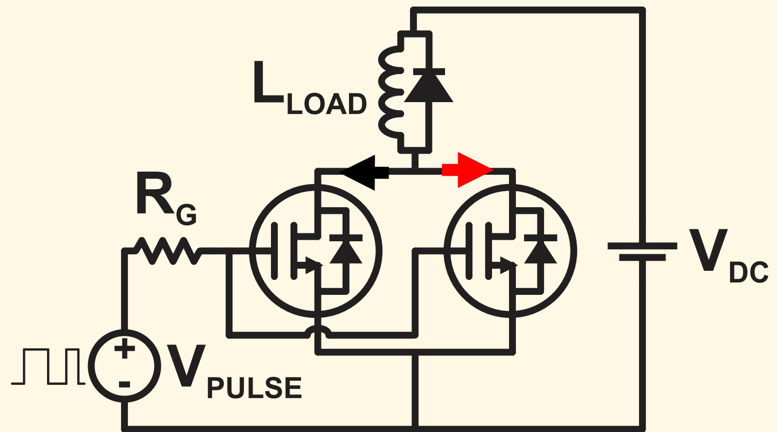


Switching transients accurately modelled both at turn-on and at turn-off

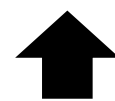
Model Validation – current imbalance

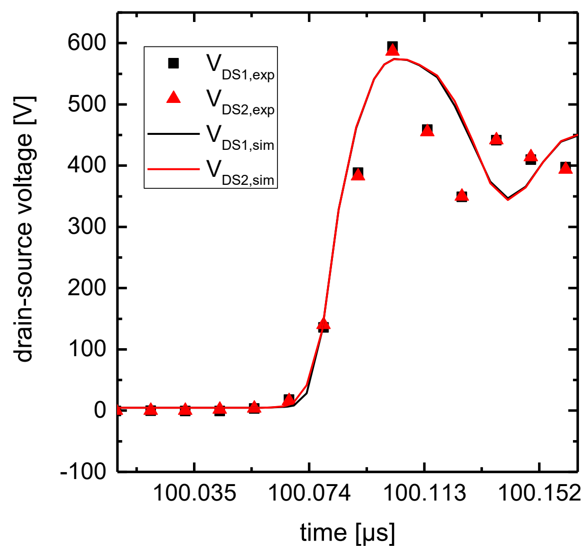
C2M0080120D

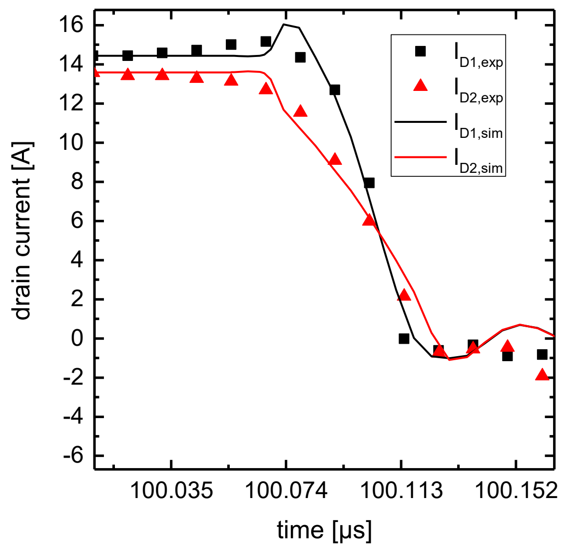
Inductive turn-off of **2 parallel SiC MOSFETs**

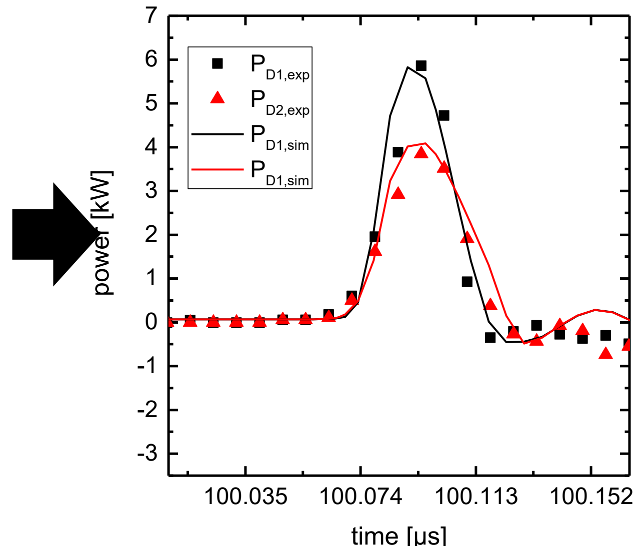


	Simulation	Experiment
MOS1	153.1 μJ	141.5 μJ
MOS2	131.8 μJ	115.05 μJ



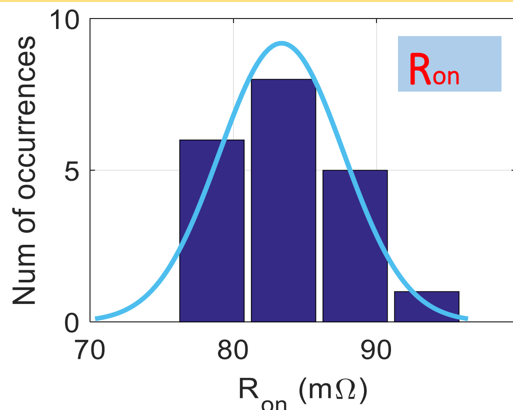


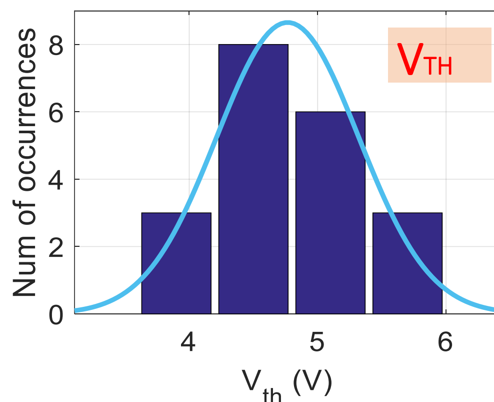




Case study: Unbalanced DCDC converter

Can the parameters mismatch represent a significant problem during realistic operation?





Histograms of statistical distribution measured on **20 DUT samples** at T=300K, and **fitting Gaussian functions**

Case study: Unbalanced DCDC converter

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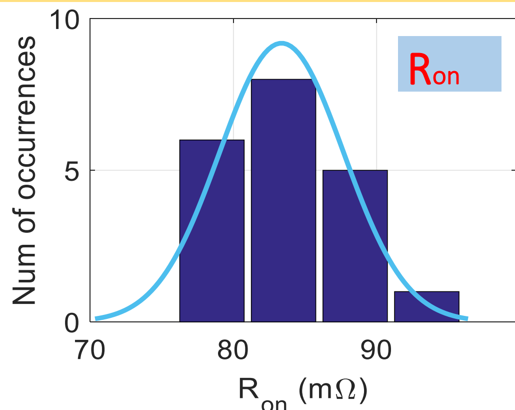
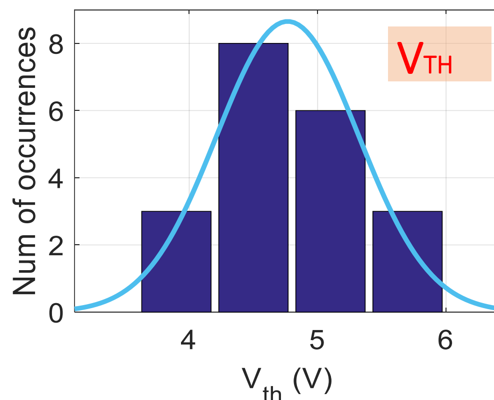
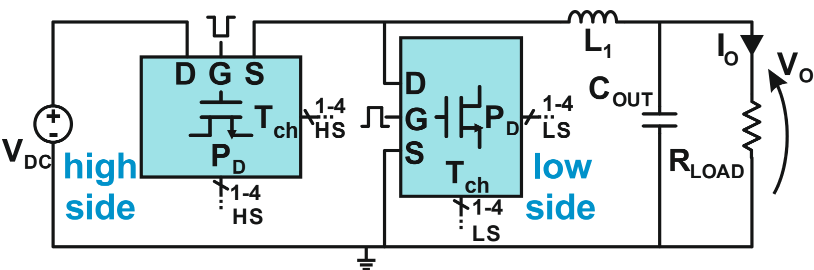




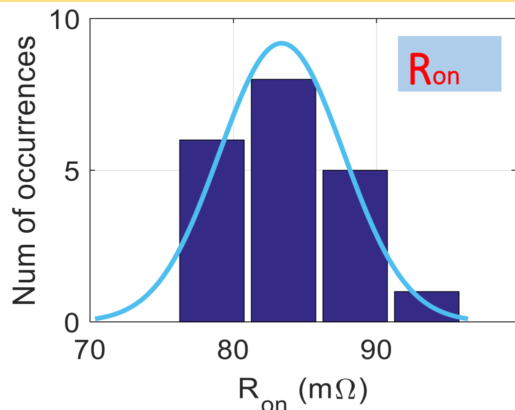
Histograms of statistical distribution measured on **20 DUT samples** at T=300K, and **fitting Gaussian functions**

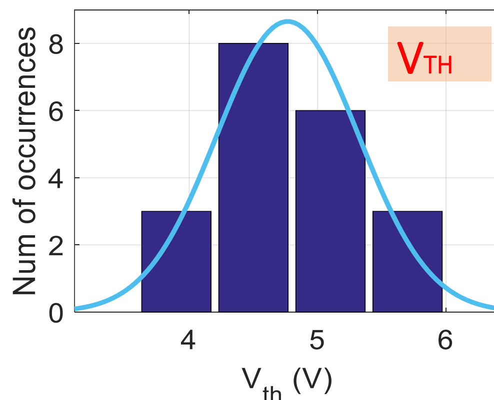


800→350 V , 200 kHz synchronous buck conv.
4 parallel MOSFETs per switch

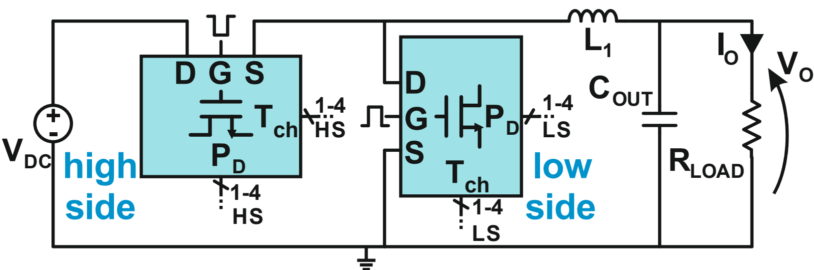
Case study: Unbalanced DCDC converter

Can the parameters mismatch represent a significant problem during realistic operation?

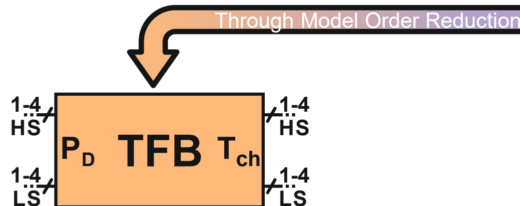


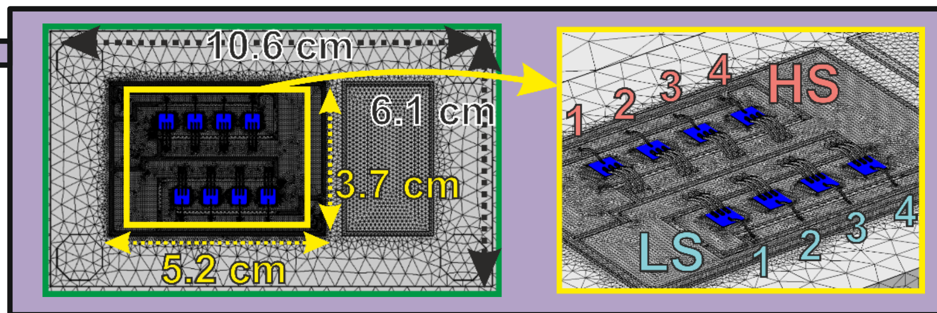


Histograms of statistical distribution measured on **20 DUT samples** at T=300K, and **fitting Gaussian functions**



800⟶350 V , 200 kHz synchronous buck conv.
4 parallel MOSFETs per switch





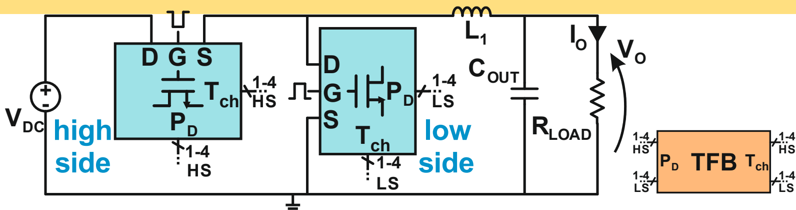
Thermal **F**eedback **B**lock

L. Codecasa *et al.*, “FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits (FANTASTIC),” in *Proc. IEEE THERMINIC*, 2014.

Case study: Unbalanced DCDC converter

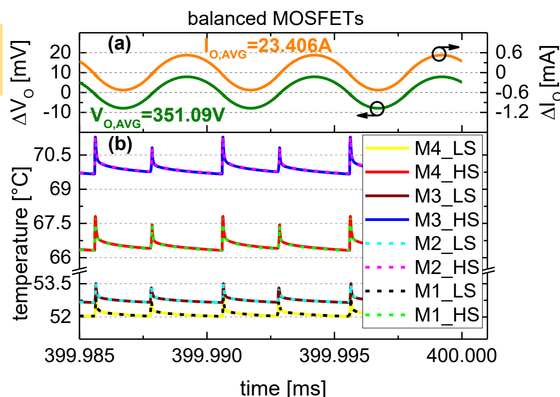
CREE
C2M0080120D

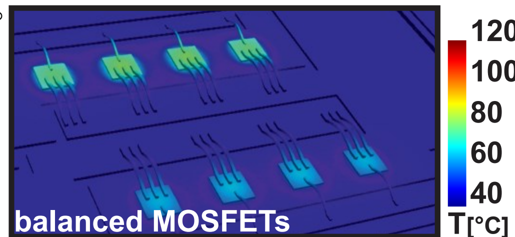
Can the parameters mismatch represent a significant problem during realistic operation?



Balanced config.

	V_{th}	K
MOS1	4.77	0.55
MOS2		
MOS3		
MOS4		

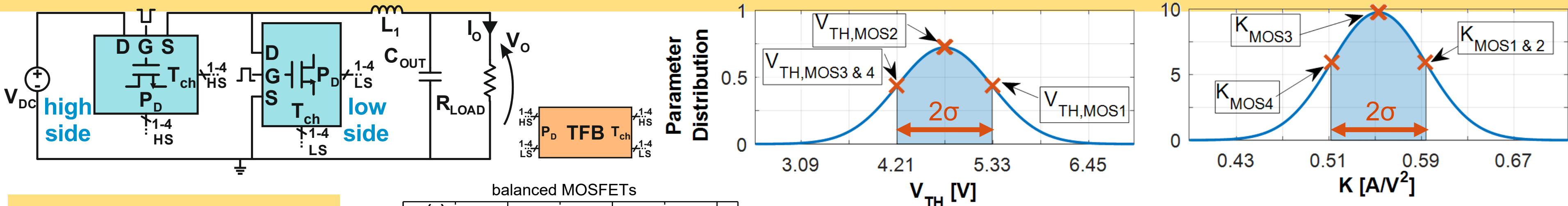




ΔT_{MAX}(balanced) ≈ 20°C

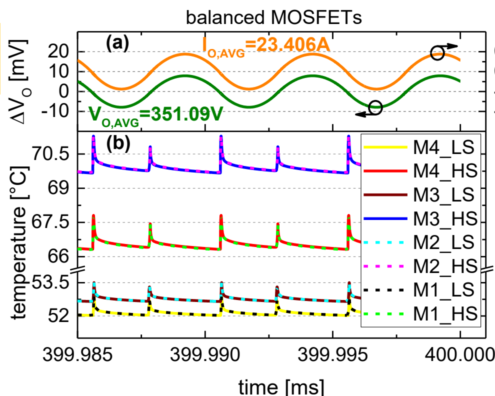
Case study: Unbalanced DCDC converter

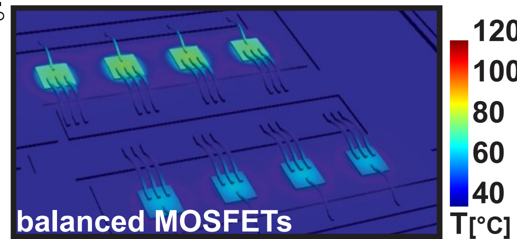
Can the parameters mismatch represent a significant problem during realistic operation?



Balanced config.

	V_{th}	K
MOS1	4.77	0.55
MOS2		
MOS3		
MOS4		



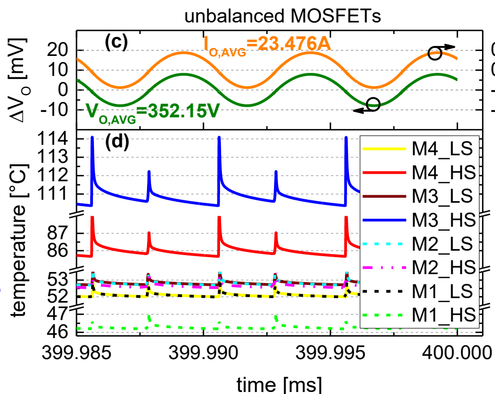


ΔT_{MAX}(balanced) ≈ 20°C

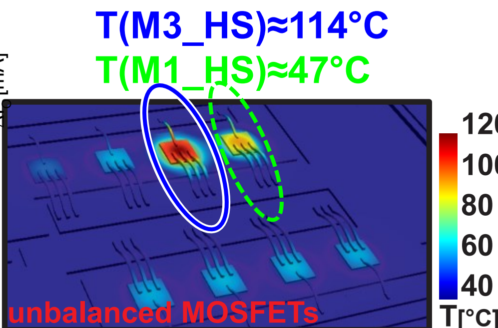
0.3% difference between Vout

unbalanced config.

	V_{th}	K
MOS1	5.32	0.59
MOS2	4.77	0.59
MOS3	4.21	0.55
MOS4	4.21	0.51



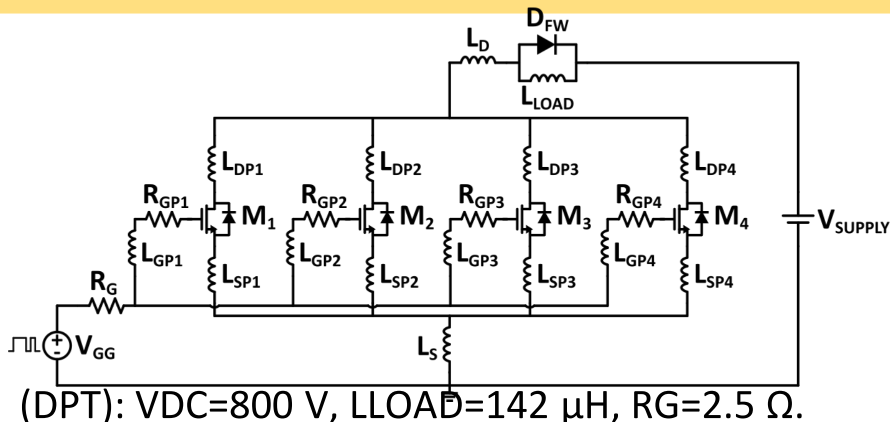
T(M3_HS)≈114°C
T(M1_HS)≈47°C



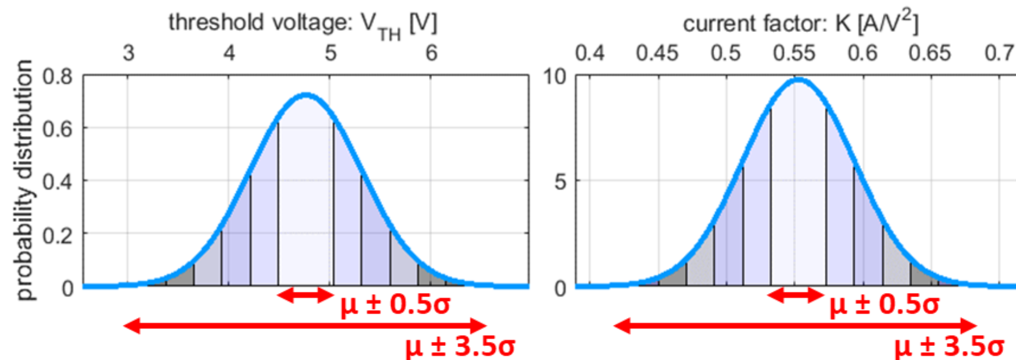
ΔT_{MAX}(unbalanced) ≈ 67°C

MONTE CARLO (MC) ANALYSIS

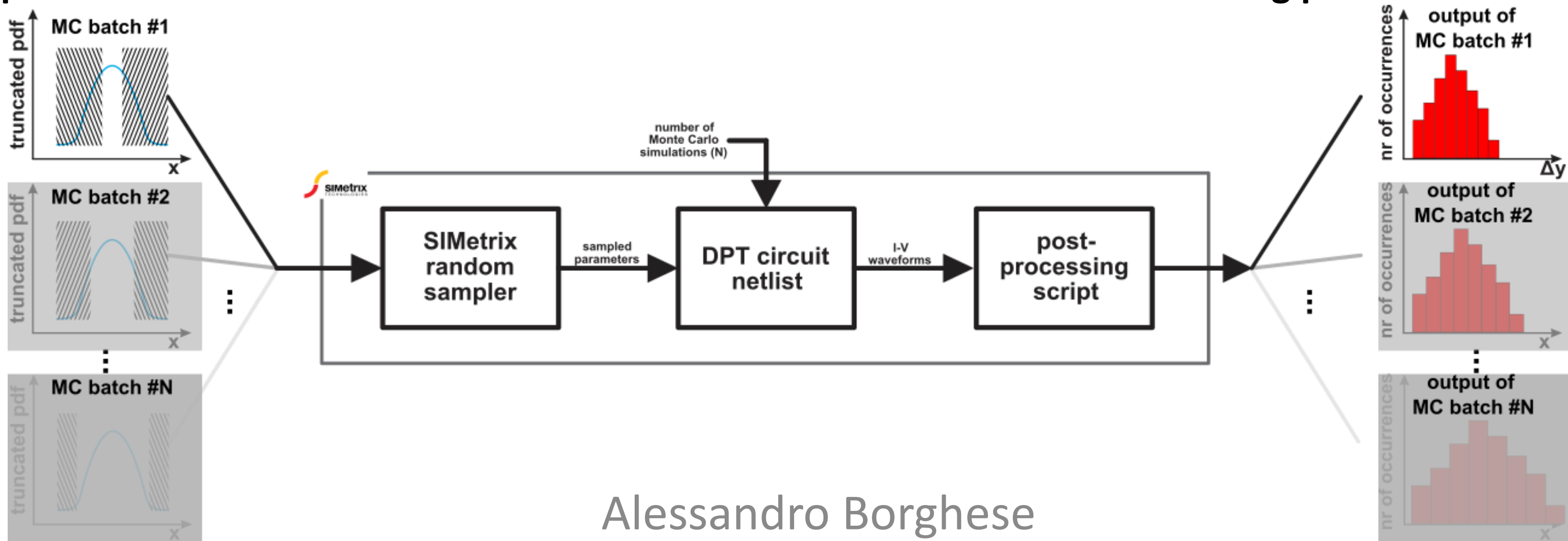
Objective: systematically relate dissipation non-uniformities of mismatched parallel devices to fabrication process rejection boundaries.



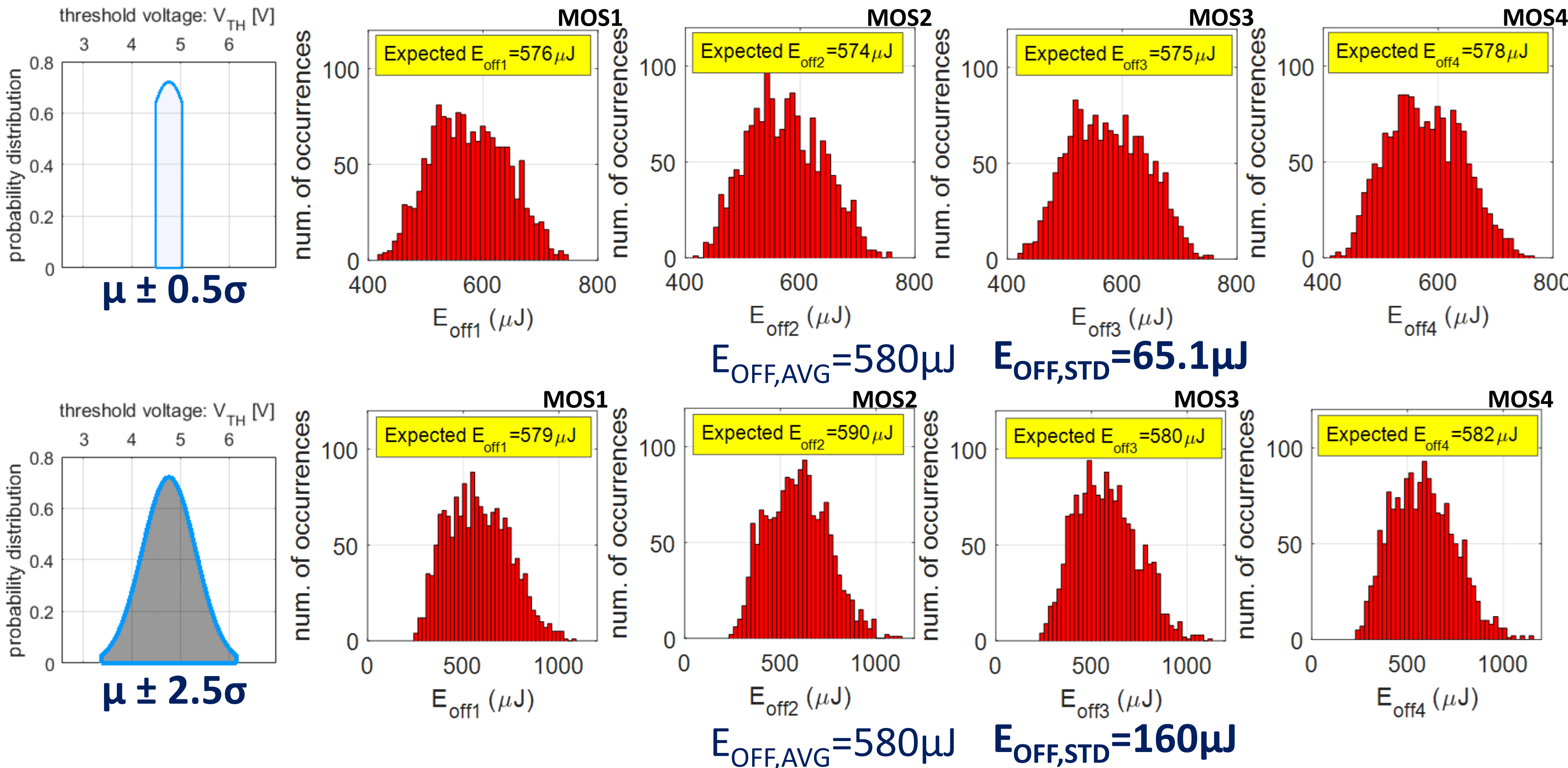
(DPT): VDC=800 V, LLOAD=142 µH, RG=2.5 Ω.



4 parallel MOSFETs under Double Pulse Test ➔ MC simulation with increasing parameters tolerances



MONTE CARLO RESULTS: TURN-OFF (example)



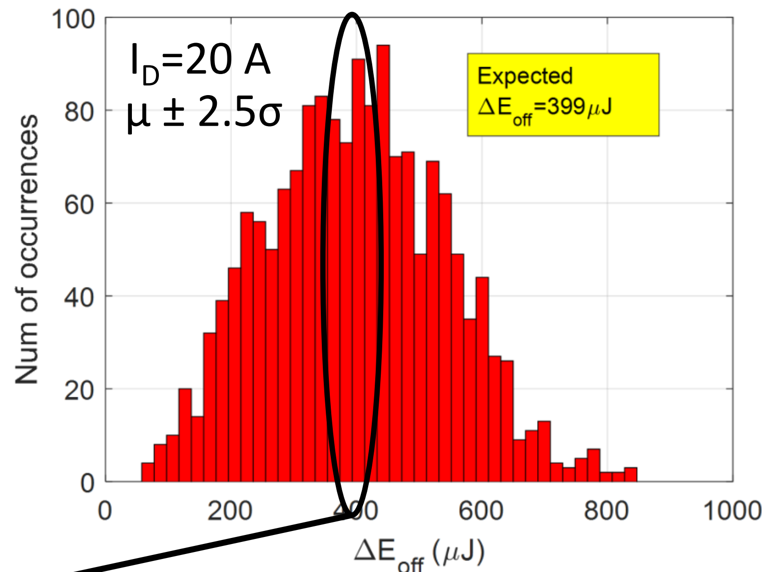
While the **mean value is constant** at 580 μJ for both cases, the **standard deviation increases from 65.1 μJ to 160 μJ.**

Statistical dissipation unbalance

- The **maximum, most likely energy unbalance,** for each MC simulation run**,** is evaluated as:

$$\Delta E_{off} = \max\left(E_{off1}, E_{off2}, E_{off3}, E_{off4}\right) - \min\left(E_{off1}, E_{off2}, E_{off3}, E_{off4}\right)$$

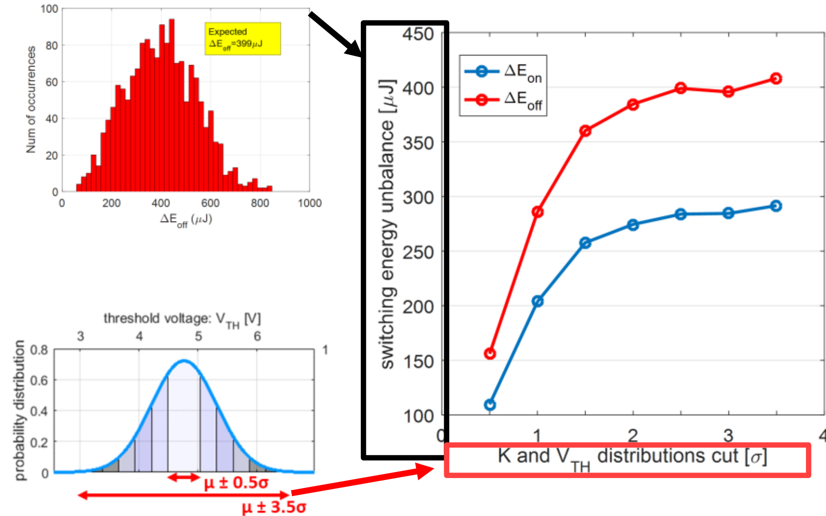
$$\Delta E_{on} = \max\left(E_{on1}, E_{on2}, E_{on3}, E_{on4}\right) - \min\left(E_{on1}, E_{on2}, E_{on3}, E_{on4}\right)$$



$\Delta E_{off,avg}$≈399μJ vs **E_{off}≈580μJ (**$\Delta E_{off}/E_{off}$ **≈69%)**

design guidelines

How to draw guidelines for the design of multi-chip power modules from these data?



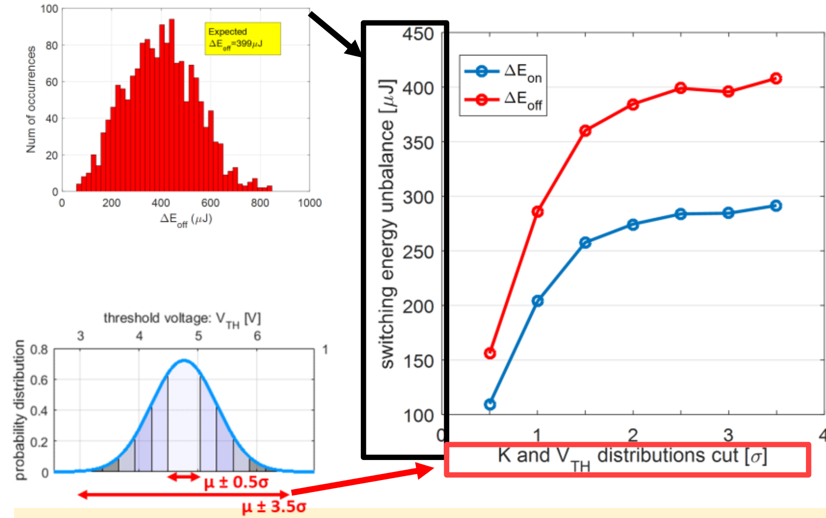
0.5

$$\Delta T = [\Delta E_{sw} \times f_{sw} + \Delta P_S \times D] \times R_{th}.$$

0.6K/W

design guidelines

How to draw guidelines for the design of multi-chip power modules from these data?



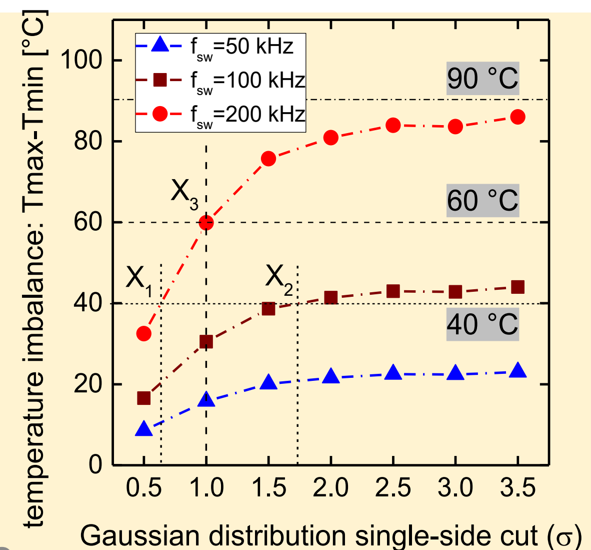
0.5

$$\Delta T = [\Delta E_{sw} \times f_{sw} + \Delta P_S \times D] \times R_{th}.$$

0.6K/W

If **ΔT_{MAX}=60°C** gives a desired **useful lifetime**

- Always achievable at 50kHz and 100kHz
- **only achievable** at 200kHz if **<u>tolerance<1σ</u>**



Summary

- A new **SPICE model** suited for **electro-thermal simulations of SiC MOSFETs.**
- **Statistical dispersions of V_{TH} and R_{ON}** for a commercial SiC power MOSFET were evaluated.
- **Monte Carlo analysis** of parallel SiC power MOSFET were performed to evaluate the **energy/temperature imbalance.**

→ **Example of design guidelines for thermal-aware design of multi-chip power module.**

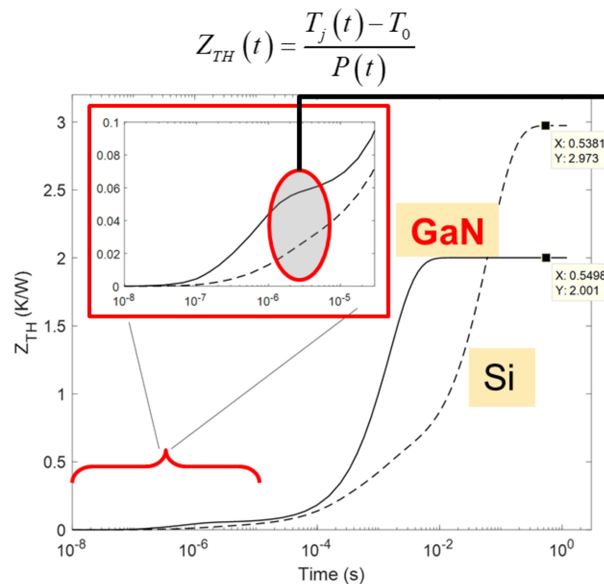
Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs

Motivation

Gallium Nitride high electron mobility transistors (GaN HEMTs) provide remarkable

- on-state (R_{on}) vs. off-state (BV) trade-off ➔ ☺ topology simplification
- switching speed ➔ ☺ more efficient and **compact** converters

↳ **Higher power density**



short-time duration events (µs scale)

$\Delta T_{GaN} = Z_{TH_{GaN}}(@2\mu s) \cdot 400V \cdot 20A(@2\mu s) \approx 440K$

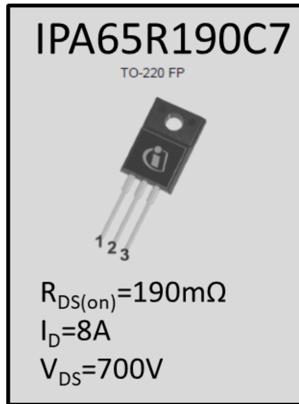
$\Delta T_{Si} = Z_{TH_{Si}}(@2\mu s) \cdot 400V \cdot 20A(@2\mu s) \approx 104K$

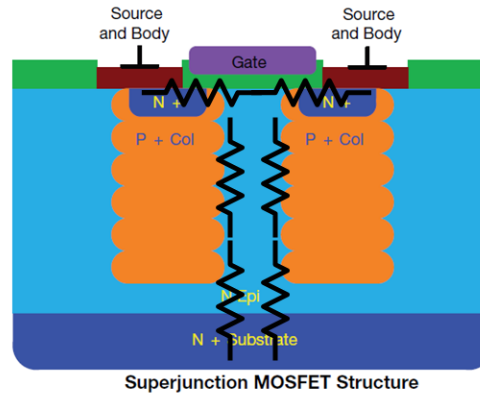
↳ **GaN faster electrothermal response**

Higher power density +
Faster thermal response =
Harsh electrothermal conditions

Online monitoring of the device self-heating is of uttermost importance

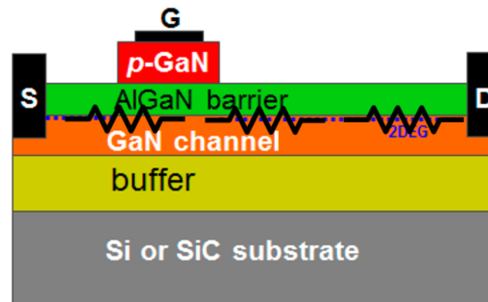
GaN faster thermal response





Superjunction MOSFET Structure

3D heat source (volume)



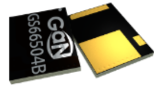
2D heat source (surface)

Very fast temperature increase

Heat generation confined in a narrow region

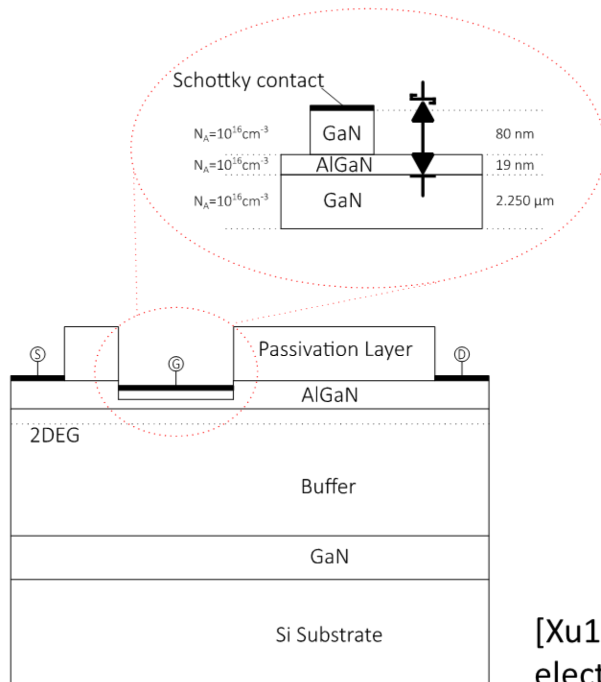
Gate Leakage Current: Physical Origin

$R_{DS(on)}$=100mΩ
I_D=15A V_{DS}=650V



GS66504B: **normally-off** p-GaN HEMTs

Gate-to-Source Current	I_{GS}	80	μA	V_{GS} = 6 V, V_{DS} = 0 V



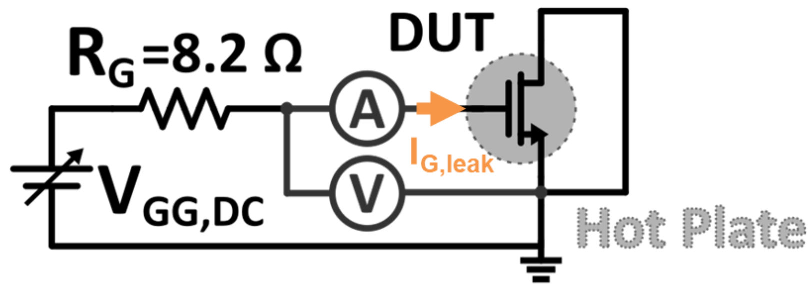
metal/p-GaN contact [Xu18]

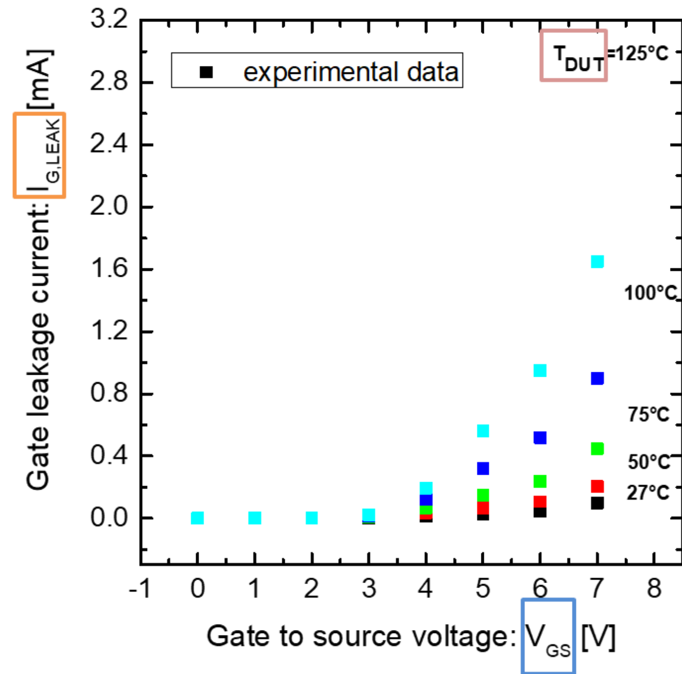
- 2-D variable range hopping
- Thermionic field emission
- Poole-Frenkle emission

[Xu18] N. Xu *et al.*, “Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors,” *Appl. Phys. Lett.*, vol. 113, no. 15, p. 152104, Oct. 2018.

Gate Leakage Current: Modelling

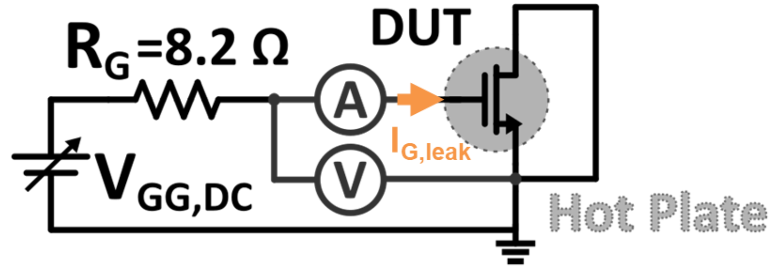
Experimental verification of the impact of V_{GS} and T_{DUT} on $I_{G,leak}$

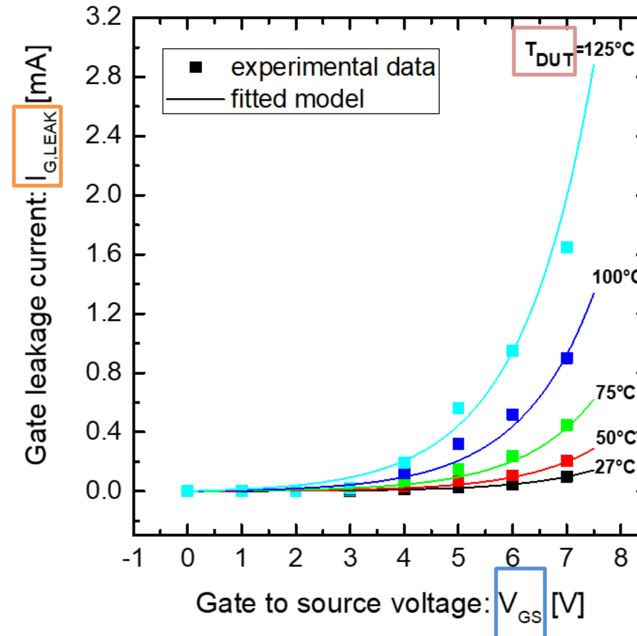




Gate Leakage Current: Modelling

Experimental verification of the impact of V_{GS} and T_{DUT} on $I_{G,leak}$





Regardless of the physical origin, $I_{G,leak}$ modelled as: $$I_{G,LEAK} = I_{G0}\left(e^{aV_{GS}} - 1\right) \cdot e^{b(T_{DUT} - T_0)} \quad (1)$$

Proposed Sensing Methodology

Instead of monitoring $I_{G,leak}$ (small and fast), we monitor the **voltage drop** (**VAK**) on the diode $\mathbf{D_{on}}$

$$I_{G,LEAK} = I_{G0}(e^{aV_{GS}} - 1) \cdot e^{b(T_{DUT} - T_0)} \quad (1)$$

$$V_{AK} = V_{GG} - V_R - V_{GS} \quad (2)$$

$$I_{G,LEAK} = I_{AK} \cong I_S e^{\frac{V_{AK}}{V_T}} \quad (3)$$

$$V_{AK} \cong V_T \left[\frac{aV_{GG} + b(T_{DUT} - T_0) - ln\left(\frac{I_S}{I_{G0}}\right)}{aV_T + 1} \right] \quad (4)$$

Advantages:

☺ **No complication of the standard gate driver**

☺ **Linear V_{AK}-T_{DUT} relation**

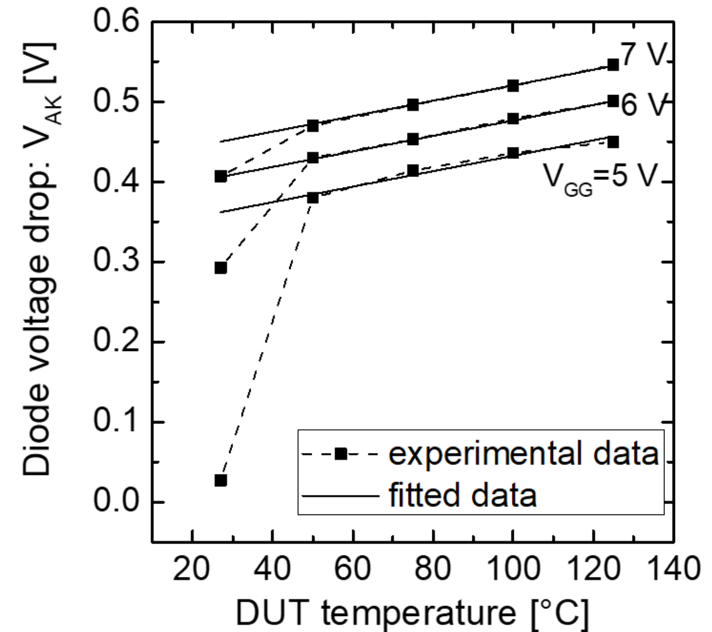
V_{AK}-T_{DUT} Relation

The linearity of $V_{AK}=f(T_{DUT})$ was experimentally verified

$$V_{AK} \cong V_T \left[\frac{aV_{GG} + b(T_{DUT} - T_0) - ln\left(\frac{I_S}{I_{G0}}\right)}{aV_T + 1} \right] \qquad (4)$$

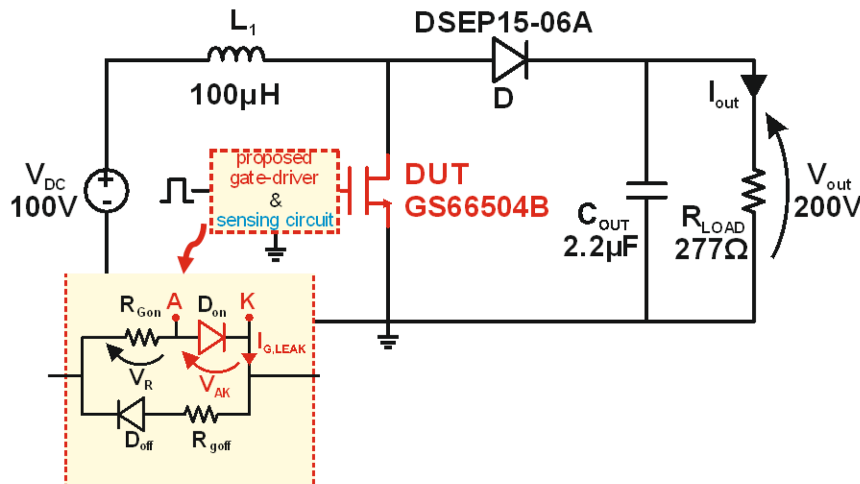
Values of the parameters used in the $V_{AK} - T_{DUT}$ relation.

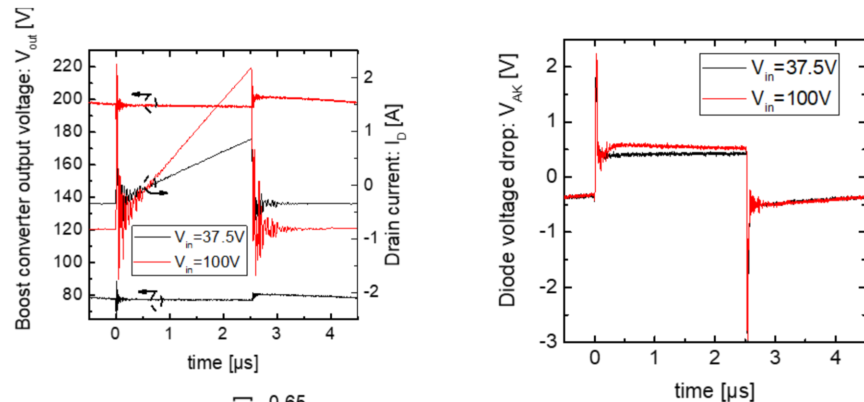
Parameter	a [V^{-1}]	b [K^{-1}]	$ln(I_S/I_{G0})$
Value	1.841	0.04033	-5.952

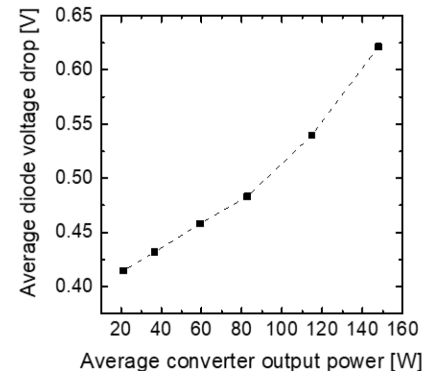


The linearity holds true for a wide range of temperature and gate bias

Sensing Methodology: Experimental Validation





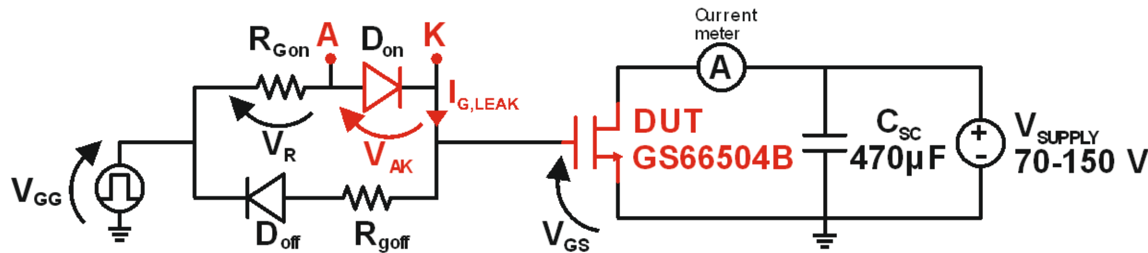


200 kHz prototype boost converter

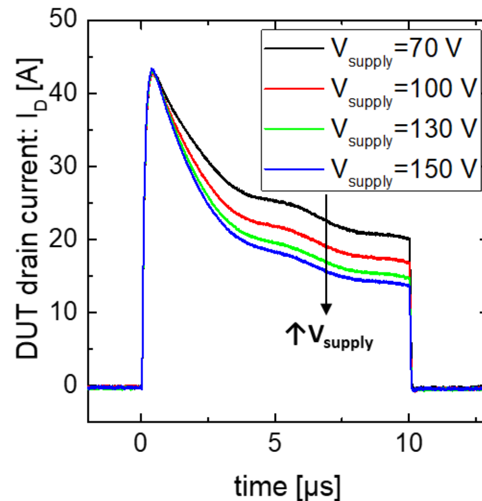
- No heatsink on the DUT to exacerbate the thermal stress
- Tested at different input voltages (V_{in}) ranging from 25 V to 100 V-, i.e., different powers.

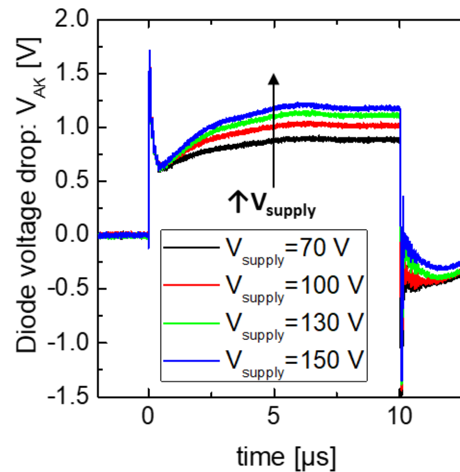
The average diode voltage drop increases as the converter output power increases

Out-of-SOA Experimental Validation



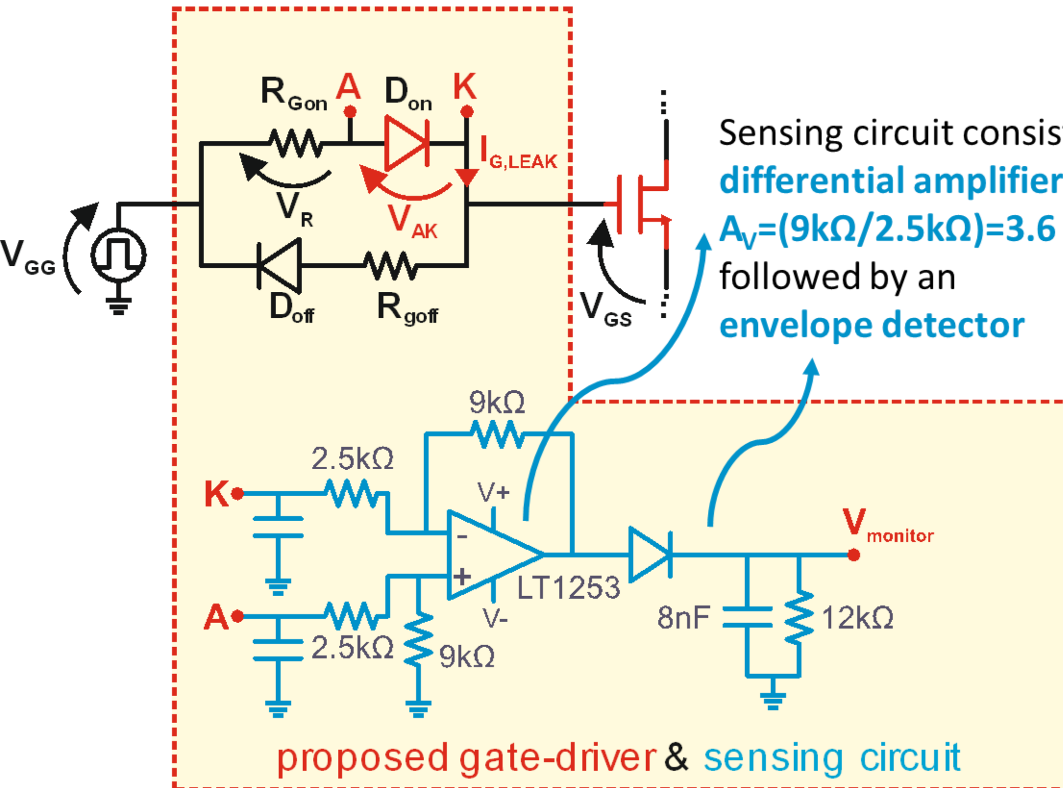
Methodology validation during **harsh operating conditions**



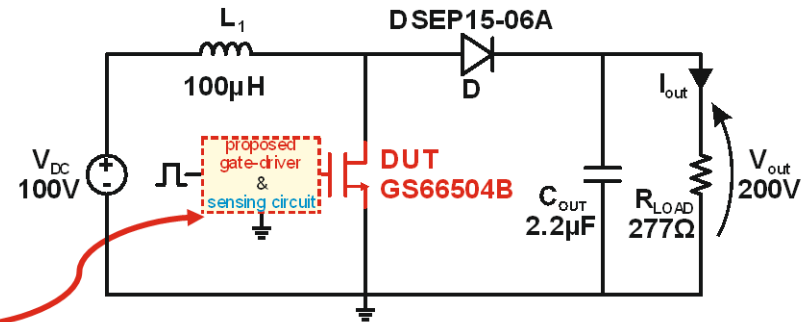


V_{AK} experienced a noticeable increase as the power dissipated by the DUT surged

V_{AK} Sensing Circuit

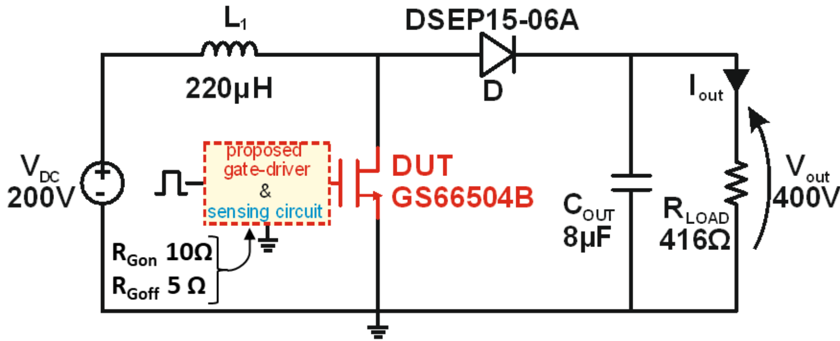


Sensing circuit consisting in **differential amplifier** **A_V=(9kΩ/2.5kΩ)=3.6** followed by an **envelope detector**



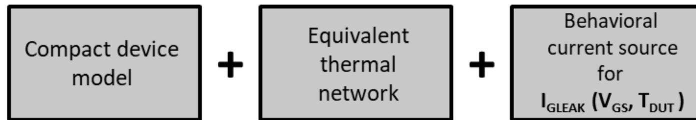
functionality tested through SPICE electrothermal simulations

V_{AK} Sensing Circuit: Validation



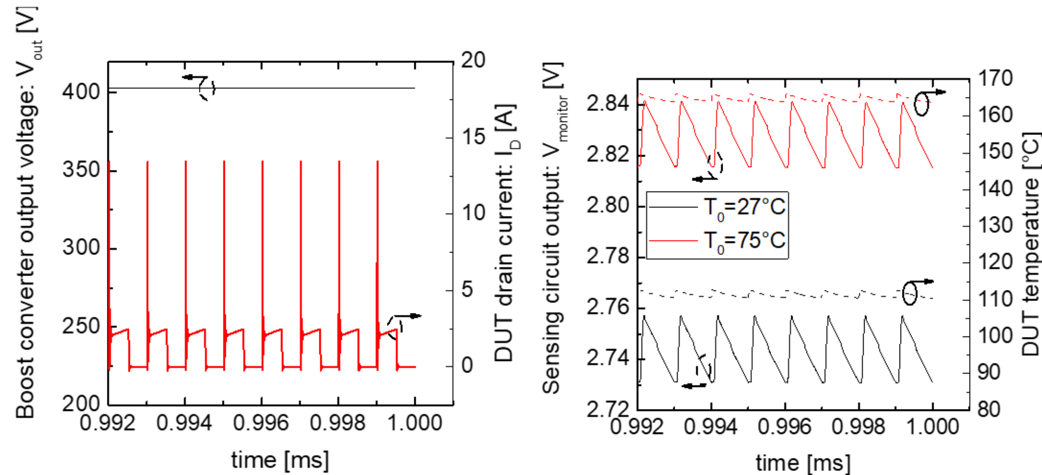
1 MHz, 200 V-to-400 V step-up converter

DUT was described by



2 electrothermal simulations at **two ambient T**

- regular operating condition T_0 = 27 °C
- stressful operating condition T_0 = 75 °C



$V_{monitor}$ has the same trend of T_{DUT} for both ambient temperatures

Summary

$I_{G,LEAK}$ as temperature indicator of GaN HEMTs investigated by experiments and simulations

- **Experimentally verified** on a **commercial GaN HEMT** that the **gate leakage current** shows a **remarkable dependence on the temperature** and on **the gate bias.** Tested both **in** and **out-of-SOA.**
- **Voltage drop across a diode on the turn-on branch of the gate driver is a good temperature equivalent parameter.**

Simple yet effective **circuit to sense and amplify the diode voltage drop was designed.**

- **Applicability tested in a 1 MHz boost converter (SPICE ET simulation).**
- **The sensing circuit does not bring an additional design burden.**

List of Publications

Journal papers (5)

A. Borghese *et al.*, "Statistical Analysis of the Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1527-1538, Sept. 2019, doi: 10.1109/JESTPE.2019.2924735.

A. Castellazzi, F. Richardeau, A. Borghese, F. Boige, A. Fayyaz, A. Irace, G. Guibaud, and V. Chazal, "Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode," *Microelectronics Reliability*, vol. 114, 2020, doi: 10.1016/j.microrel.2020.113943.

A. Borghese, M. Riccio, G. Longobardi, L. Maresca, G. Breglio, and A. Irace, "Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs," *Microelectronics Reliability*, vol. 114, 2020, doi: 10.1016/j.microrel.2020.113762.

A. Borghese, A. D. Costanzo, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate current in p-GaN gate HEMTs as a channel temperature sensitive parameter: A comparative study between schottky-and ohmic-gate GaN HEMTs," *Energies*, vol. 14, no. 23, 2021, doi: 10.3390/en14238055.

C. Scognamillo, A. P. Catalano, M. Riccio, V. d'Alessandro, L. Codecasa, A. Borghese, R. N. Tripathi, A. Castellazzi, G. Breglio, and A. Irace, "Compact modeling of a 3.3 kV SiC MOSFET power module for detailed circuit-level electrothermal simulations including parasitics," *Energies*, vol. 14, no. 15, 2021, doi: 10.3390/en14154683.

Book chapters (2)

L. Maresca, A. Borghese, G. Romano, A. Fayyaz, M. Riccio, G. Breglio, A. Castellazzi, and A. Irace, "SiC MOSFETs," in *Modern Power Electronic Devices*, 2020, pp. 259–293. doi: 10.1049/PBPO152E_ch8.

M. Riccio, A. Borghese, V. d'Alessandro, L. Maresca, and A. Irace, "Optimum module design II: impact of parameter design spread," in *SiC Power Module Design: Performance, Robustness and Reliability*, 2021, pp. 107–132.

Conference papers (10)

M. Riccio, A. Borghese, G. Romano, V. d'Alessandro, A. Fayyaz, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, "Analysis of Device and Circuit Parameters Variability in SiC MOSFETs-Based Multichip Power Module," 2018. [Online]. Available: https://www.scopus.com/inward/record.uri?eid=2-s2.0-85057005975&partnerID=40&md5=1602372b3901fa7b4b9e62ca133596eb

A. Borghese *et al.*, "Effect of Parameters Variability on the Performance of SiC MOSFET Modules," *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1-5, doi: 10.1109/ESARS-ITEC.2018.8607593.

M. Riccio, G. Romano, A. Borghese, L. Maresca, G. Breglio A. Irace, and G. Longobardi, "Experimental analysis of electro-thermal interaction in normally-off pGaN HEMT devices," *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1-6, doi: 10.1109/ESARS-ITEC.2018.8607347.

A Borghese *et al.*, "An Experimentally Verified 3.3 kV SiC MOSFET Model Suitable for High-Current Modules Design," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2019, vol. 2019-May, pp. 215–218. doi: 10.1109/ISPSD.2019.8757576.

M. Riccio, A. Borghese, L. Maresca, G. Breglio and A. Irace, "Fully-Coupled Electrothermal Simulation of Wide-Area Reverse Conducting IGBTs," *2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2019, pp. 1-4, doi: 10.1109/THERMINIC.2019.8923497.

F. Richardeau F. Boige, A. Castellazzi, V. Chazal, A. Fayyaz, A. Borghese, A. Irace, and G. Guibaud, "SiC MOSFETs soft and hard failure modes: Functional analysis and structural characterization," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2020, vol. 2020-September, pp. 170–173. doi: 10.1109/ISPSD46842.2020.9170094.

A. Borghese, M. Riccio, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, "Statistical Electrothermal Simulation for Lifetime Prediction of Parallel SiC MOSFETs and Modules," in *Proceedings - 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems, IESES 2020*, 2020, pp. 383–386. doi: 10.1109/IESES45645.2020.9210690.

F. Richardeau, A. Borghese, A. Castellazzi, A. Irace, V. Chazal, and G. Guibaud, "Effect of gate-source bias voltage and gate-drain leakage current on the short-circuit performance of FTO-type SiC power MOSFETs," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 255–258. doi: 10.23919/ISPSD50666.2021.9452253.

C. Scognamillo, A. P. Catalano, A. Borghese, M. Riccio, V. d'Alessandro, G. Breglio, A. Irace, R. N. Tripathi, A. Castellazzi, and L. Codecasa, "Electrothermal Modeling, Simulation, and Electromagnetic Characterization of a 3.3 kV SiC MOSFET Power Module," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 123–126. doi: 10.23919/ISPSD50666.2021.9452207.

A. Borghese, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate Driver for p-GaN HEMTs with Real-Time Monitoring Capability of Channel Temperature," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 63–66. doi: 10.23919/ISPSD50666.2021.9452317.

ECTS summary

Student: Alessandro Borghese alessandro.borghese@unina.it
Tutor: Andrea Irace andrea.irace@unina.it
Cycle XXXIV

	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0.4	5		11	5		**22**	10			5	4			**9**	0					2.5		**2.5**	**33**	**30-70**
Seminars	5			1.1	4.8			**5.9**	6	0.4		0.4	1.5		3.7	**6**	0							**0**	**12**	**10-30**
Research	35	9.6	5	8.9	0	5	10	**39**	45	9.6	10	4.6	4.5	10	6.3	**45**	60	10	10	10	10	7.5	10	**58**	**141**	**80-140**
	60	10	10	10	16	10	10	**66**	61	10	10	10	10	10	10	**60**	60	10	10	10	10	10	10	**60**	**186**	**180**

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