PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Alessandro Borghese

XXXIV Cycle

Training and Research Activities Report – Third Year

Tutor: Prof. Andrea Irace

Add the following items according to our meeting we have.

Concerning the structure of the document, use the Section number as is. Use the sub-contents indicated with a letter only as a suggestion for your content (a free form text is preferable)

1. Information

Alessandro Borghese received his BSc and MSc degrees in electronic engineering from the University of Naples Federico II. On October 23rd, 2017, he defended the master thesis entitled "Efficiency Estimation and Comparison of Two Inverters for Electric Vehicles: Si vs. SiC Power Devices". The thesis activity was developed as a part of a one-year internship at the Technical Centre of Toyota Motor Europe (Hoge Wei 33, B-1930 Zaventem, Belgium).
After his graduation, Mr. Borghese worked at the Electrothermal Characterization Laboratory (Dept. of Electrical Engineering and Information Technology - Building 2 -, University of Naples Federico II, Via Claudio 21, Naples) from November 2017 to October 2018.
On October 2018, Mr. Borghese took part in the public admission procedure for enrolling at the Information Technology and Electrical Engineering PhD of the University of Naples Federico II. He was awarded with a ministerial scholarship and officially started the 34th PhD cycle on November 1st under the tutorship of Prof. Andrea Irace.
Mr Borghese's research activity is focused on power electronics and it specifically concerns the study of wide bandgap power semiconductor devices.

2. Study and Training activities
During the third year, Alessandro Borghese attended the following courses:

   a. Courses
      - "Real-Time Embedded Systems for IIoT and I4.0" – Alessandro Cilardo, Marcello Cinque – 07/2022 (2.5 ECTS)

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	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0.4	5		11	5		22	10			5	4			9	0					2.5		2.5	33	30-70
Seminars	5			1.1	4.8			5.9	6	0.4		0.4	1.5		3.7	6	0							0	12	10-30
Research	35	9.6	5	8.9	0	5	10	39	45	9.6	10	4.6	4.5	10	6.3	45	60	10	10	10	10	7.5	10	58	141	80-140
	60	10	10	10	16	10	10	66	61	10	10	10	10	10	10	60	60	10	10	10	10	10	10	60	186	180

3. Research activity
   1. SiC MOSFETs.
      1.1. Compact modelling SiC power MOSFETs for performing fully-coupled electrothermal simulations entirely within SPICE environment.
      1.2. Investigation of a type of short-circuit failure that is interesting for the parallel connection of SiC MOSFETs. This failure mode results in a MOSFET with a partial short circuit between

gate and source but that still retains the capability of blocking the current between drain and source.

1.3. Study of the impact of parameters spread on the electrothermal imbalances in parallel SiC MOSFETs. Several relevant parameters, device- or assembly-related, have been studied and, for each of them, the impact on the imbalance of static power dissipation, switching energy, and transient current sharing has been investigated. Exploiting Monte Carlo simulations, a procedure to derive a trade-off curve between the parameters spread and the temperature imbalance has been also developed.

2. Study on the gate current of p-Gate GaN HEMTs.
   2.1. Discussion on the requirements of the gate-driver circuit for the two different classes of normally-off GaN HEMTs with p-type gate;
   2.2. Assessment of the viability of using the gate current as a temperature-sensitive electrical parameter (TSEP) and proposing a sensing circuit for its online monitoring.
3. Study and development of Si and SiC power diodes through TCAD simulations performed in Synopsys-Sentaurus. This activity has been conducted in partnership with VISHAY Semiconductors and, because of confidentiality constraints, did not result in publications.

   Study of the performance of an α-type Ga_2O_3 SBD in a real application. The results offer a preliminary indication that the device fully meets the main expectations associated with the technology, namely: very fast switching; very contained reverse current flow during turn-off; very stable temperature performance.

4. Products
   a. Publications

- F. Richardeau, **A. Borghese**, A. Castellazzi, A. Irace, V. Chazal, and G. Guibaud, "Effect of gate-source bias voltage and gate-drain leakage current on the short-circuit performance of FTO-type SiC power MOSFETs," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 255–258. doi: 10.23919/ISPSD50666.2021.9452253.

- C. Scognamillo, A. P. Catalano, **A. Borghese**, M. Riccio, V. d'Alessandro, G. Breglio, A. Irace, R. N. Tripathi, A. Castellazzi, and L. Codecasa, "Electrothermal Modeling, Simulation, and Electromagnetic Characterization of a 3.3 kV SiC MOSFET Power Module," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 123–126. doi: 10.23919/ISPSD50666.2021.9452207.

- **A. Borghese**, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate Driver for p-GaN HEMTs with Real-Time Monitoring Capability of Channel Temperature," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 63–66. doi: 10.23919/ISPSD50666.2021.9452317.

- **A. Borghese**, A. D. Costanzo, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate current in p-GaN gate HEMTs as a channel temperature

sensitive parameter: A comparative study between schottky-and ohmic-gate GaN HEMTs," *Energies*, vol. 14, no. 23, 2021, doi: 10.3390/en14238055.

- C. Scognamillo, A. P. Catalano, M. Riccio, V. d'Alessandro, L. Codecasa, **A. Borghese**, R. N. Tripathi, A. Castellazzi, G. Breglio, and A. Irace, "Compact modeling of a 3.3 kV SiC MOSFET power module for detailed circuit-level electrothermal simulations including parasitics," *Energies*, vol. 14, no. 15, 2021, doi: 10.3390/en14154683.

- M. Riccio, **A. Borghese**, V. d'Alessandro, L. Maresca, and A. Irace, "Optimum module design II: impact of parameter design spread," in *SiC Power Module Design: Performance, Robustness and Reliability*, 2021, pp. 107–132.

5. Conferences and Seminars
   a. 2021 IEEE 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya (online), Japan, 05/30-03/06 2021.
      → 3 papers, 1 poster presentation 1 oral presentation.
   b. 2021 IEEE 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya (online), Japan, 05/30-03/06 2021.
      → 3 papers, 1 poster presentation 1 oral presentation.
   c. 13th European Conference on Silicon Carbide and Related Materials (ECSCRM), Tours, France, 24-28/10 2021.
      → 1 paper, 1 oral presentation.
   d. 2021 Meeting Annuale Società Italiana di Elettronica (SIE), Trieste, 2021.
      → 1 paper, 1 oral presentation.

6. Activity abroad

Year	Institution	Responsible for the foreign institution	Dates	Performed activities
3	SP2-Lab, Faculty of Engineering, Kyoto University of Advanced Science, Kyoto, Japan	Alberto Castellazzi, Full Professor	09/12/2020-13/06/2021	1) Study of the performance of an α-type Ga_2O_3 SBD in a real application. The results offer a preliminary indication that the device fully meets the main expectations associated with the technology, namely: very fast switching; very contained reverse current flow during turn-off; very stable temperature performance. 2) Study on the performance of GaN-based half bridges with integrated gate driver.

7. Tutorship
   a. Co-supervision of MSc student (Pio Nicola Di Costanzo) thesis on "Analisi e caratterizzazione sperimentale di un circuito di monitoraggio della temperatura di canale per dispositivi P-GaN gate HEMTs in applicazioni di convertitori switching".

b. Co-supervision of MSc student (Domenico Russo) thesis on “Caratterizzazione sperimentale e modellistica compatta di SiC Power MOSFET da 1.7 kV”.
c. Elettronica per l’industria, BSc in mechatronic engineering:
    - 2021/11/23 (2 hours) – Exame practice
    - 2021/11/24 (2 hours) – Exame practice
    - 2021/12/07 (2 hours) – Exame practice