PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Alessandro Borghese

XXXIV Cycle

Training and Research Activities Report – Second Year

Tutor: Prof. Andrea Irace

1. Information

Alessandro Borghese received his BSc and MSc degrees in electronic engineering from the University of Naples Federico II. On October 23rd, 2017, he defended the master thesis entitled "Efficiency Estimation and Comparison of Two Inverters for Electric Vehicles: Si vs. SiC Power Devices". The thesis activity was developed as a part of a one-year internship at the Technical Centre of Toyota Motor Europe (Hoge Wei 33, B-1930 Zaventem, Belgium).
After his graduation, Mr. Borghese worked at the Electrothermal Characterization Laboratory (Dept. of Electrical Engineering and Information Technology - Building 2 -, University of Naples Federico II, Via Claudio 21, Naples) from November 2017 to October 2018.
On October 2018, Mr. Borghese took part in the public admission procedure for enrolling at the Information Technology and Electrical Engineering PhD of the University of Naples Federico II. He was awarded with a ministerial scholarship and officially started the 34th PhD cycle on November 1st under the tutorship of Prof. Andrea Irace.
Mr Borghese's research activity is focused on power electronics and it specifically concerns the study of wide bandgap power semiconductor devices.

2. Study and Training activities

During the second year, Alessandro Borghese attended several courses and seminars to expand his knowledge in different areas. A full list of the training activities undertaken by Mr. Borghese is reported below:

- Courses
  - "Scientific Programming and Visualization with Python" – Dr. Alessio Botta – 27-28/02/2020 (3 ECTS)
  - "Matlab Fundamentals" – Dr. Stefano Marrone – 27/03/2020 (2 ECTS).
  - "Virtualization technologies and their applications" – Dr. Luigi De Simone – 06/04/2020 to 15/05/2020 (4 ECTS).
- Seminars
  - "Lo spazio cibernetico come dominio bellico", Prof. Guglielmo Tamburrini, 15/11/2019 (0.4 ECTS).
  - "How to Get Published with IEEE", Eszter Lukacs, 20/04/2020 (0.4 ECTS).
  - "Access the eLearning Library", Eszter Lukacs, 04/05/2020 (0.2 ECTS).
  - "Large Scale Training of Deep Neural Networks", Prof. Carlo Sansone, 06/05/2020 (0.5 ECTS).
  - "Plasmonica ON Line – Sensing", Prof. Maria Cateria Giordano et. al., 20/05/2020 (0.8 ECTS). http://www.plasmonica.it/
  - "Topics on Microelectronics (ToM)", Prof. Andrea Baschirotto, 08 – 12/09/2020 (3.5 ECTS). http://www.innotechevents.com/index.php?page=ToM/ToM.html
  - "IEEE *Xplore*® Digital Library", Dr Alessandra Scippa, 23/09/2020 (0.2 ECTS).

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	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0.4	5		11	5		22	10			5	4			9	0							0	31	30-70
Seminars	5			1.1	4.8			5.9	6	0.4		0.4	1.5		3.7	6	0							0	12	10-30
Research	35	9.6	5	8.9	0	5	10	39	45	9.6	10	4.6	4.5	10	6.3	45	60							0	84	80-140
	60	10	10	10	16	10	10	66	61	10	10	10	10	10	10	60	60	0	0	0	0	0	0	0	126	180

3. Research activity

Introduction

Mr Borghese's research activity falls in the field of power electronics and, specifically, it focuses on the study of wide bandgap (WBG) power semiconductor devices.

The field of power electronics focuses on the use of solid-state electronic devices for the conversion, control, and processing of electricity and electric power. Silicon (Si) semiconductors have traditionally been employed in fabricating these power circuits. However, as devices and equipment evolve and become more powerful, existing Si power electronics are losing the ability to keep pace with increasing performance demands. This is primarily attributed to the fact that traditional Si device technology has matured to a point where it is pushing the fundamental limitations of this material system. Wide bandgap (WBG) semiconductors have shown the capability to meet the higher performance demands of the evolving power equipment, operating at higher voltages and temperatures and enabling switching frequencies with greater efficiencies compared with existing Si devices. Along with performance improvements, WBG-based power electronics can be fabricated with a much smaller footprint (reduced volume) compared with similarly rated Si devices due to decreased cooling requirements and smaller passive components, contributing to overall lower system costs.

WBG semiconductors are materials (elements or compounds) whose bandgap (energy difference between valence and conduction bands) is bigger than 1.12 eV, which is the silicon (Si) bandgap value. Two major WBG materials with the potential to enable significant advances in power electronics are silicon carbide (SiC) and gallium nitride (GaN). While SiC currently has limited use in power electronics, its role is expected to grow as it becomes the prevailing WBG replacement for Si in applications requiring device ratings exceeding 600 volts. A major challenge to widespread adoption of SiC power electronics devices is the high cost of substrates and epitaxial materials. These high costs are tied to small production volumes and high manufacturing costs. Significant markets are expected for SiC devices in hybrid and electric vehicles as well as solar inverters and power supplies. SiC diodes are already used with companion Si transistors in photovoltaic (PV) inverters and hybrid vehicle chargers. Their greatest revenue-generating applications are expected to be in industrial motor drives and hybrid and electric vehicles.

GaN is currently widely used in LEDs and radio frequency (RF) amplifiers, and its emergence in power electronics is relatively recent. Challenges for GaN-on-Si semiconductors, the current most cost-effective method for fabricating GaN power devices, are mostly related to their lack of maturity. Issues include overcoming material challenges, such as the high lattice strain at the GaN and Si interface owing to mismatches in the coefficient of thermal expansion. GaN high-electron-mobility transistors (HEMTs) are expected to be the dominant WBG semiconductor replacement for Si in applications requiring device ratings less than 600 V.

Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs

Over the past 2 decades, the adoption of silicon carbide (SiC) metal oxide field effect transistors (MOSFETs) noticeably surged. This growing diffusion can be mainly attributed to the development and subsequent commercialization of devices with exceptional static and dynamic characteristics. Despite featuring performances that are superior to those of their silicon (Si) counterparts, the current rating of state of the art 1.2 kV SiC MOSFETs does not exceed 120 A. This limits the variety of applications where such devices can be adopted, thus intensifying the need for paralleling multiple chips to achieve higher current levels. However, during the design of an array of parallel semiconductor devices, whether this is implemented at the module level (i.e., by connecting together various chips within the same package) or at circuit level (i.e., by wiring a number of discrete devices on the same circuit board), special care must be taken to mitigate the current imbalance among the parallel units. For SiC power modules, the uneven current sharing can be caused both by mismatches in inherent device parameters and by assembly-related asymmetries. Although these sources of uncertainty are present also when paralleling Si devices, their effect is made more prominent for SiC due to a less mature technological process (leading to bigger parameters fluctuations) and faster switching transients (exacerbating the effects associated to stray elements).

Several inherent device properties, such as ON-state resistance R_{ON}, threshold voltage V_{TH}, transconductance g_m, breakdown voltage V_{BR}; as well as assembly related electrothermal (ET) and

electromagnetic (EM) mismatches can lead to nonuniform static and dynamic performances. Furthermore, the performance spread may vary over time as the parameters shift with the temperature and device ageing. Therefore, some devices might endure an overstress undermining the lifetime or the reliability of the whole assembly. Consequently, developing design guidelines and derating rules is essential for the optimization of parallel configurations of SiC MOSFETs. To do so, an indispensable in-depth comprehension of the influence of the parameters spread on the performances of the devices must first be achieved. Some early examples of analysis of the criticalities regarding the parallel connection of unipolar SiC devices and the parameters affecting them can be found in literature. Further studies, more specifically focused on SiC MOSFETs, have been conducted on the pivotal parameters leading to unbalanced current sharing, both at experimental level and simulation level. Other articles explore the effects of asymmetrical circuit design, either exclusively or in conjunction with imbalances in device parameters. In addition, the impact of unequal parasitic inductances on the current imbalance between body diodes of parallel SiC MOSFETs has been examined as well in literature. Some studies inspecting the adoption of parallel SiC MOSFETs in power electrical converters have also been published. In a literature example where a converter is switched at 100 kHz, it is found that the unbalanced switching losses can cause thermal runaway. Consequently, since the operation at high switching frequencies is highly desirable to reduce the system volume, the containment of loss spread is of paramount importance. To do so, several approaches have been proposed in the literature: some of them consist in active balancing techniques while others rely on passive components or layout optimization. Moreover, given a current derating factor, a methodology to select the admissible spread of R_{ON} and V_{TH} has been developed too. In addition to this, the robustness of parallel SiC multichip structures has been analyzed under both unclamped and clamped inductive switching. Despite the number of publications discussing balancing methods and derating rules, none of them is based on a statistical derivation. The latter is of paramount importance, especially when selecting safety margins, as worst-case assumptions tend to overestimate the derating factors. Since SiC devices are still expensive when compared to equally rated Si devices, it is of great interest to minimize the derating requirements. Therefore, the statistical description of parameters variability become a key approach to develop a methodology for deriving a design guideline for the safe operation of parallel SiC devices. The selected key quantities for the statistical analysis are device intrinsic features (e.g. MOSFET current factor K, threshold voltage V_{TH}, MOSFET capacitances C_{GS}, C_{GD} and C_{DS}, etc.) and circuit parameters such as gate resistance (R_{GP}) and source inductance (L_{SP}).

To perform the aforementioned analysis, it is required to use an accurate, yet reliable, device compact model to carry out circuit simulations in a large variety of scenarios.

In the last years, several papers have been focused on the modeling of SiC MOSFETs. Many works start from models developed for Si MOSFETs and enrich them with various parameters and empirical functions to reproduce the characteristics of the SiC counterparts. However, models based on an empirical formulation of the device behavior result in an onerous and prone-to-error calibration procedure. Recently, some models have been published with the aim to describe the specific mechanisms occurring in SiC MOSFETs. Various sophisticate physical models have been developed for device simulations, but in many cases, they are too resource-hungry to be exploited for the analyses of complex circuits. The model used in this study is an accurate, yet simple enough, physics-based model, which is associated to a straightforward parameter extraction methodology. Such model is oriented to ET simulation in real applications (e.g., power converters) with the possibility to enable physical phenomena occurring close to the device failure.

The model is implemented as a sub-circuit fully compatible with most commercial SPICE-like software suites and can be solved by their powerful engines with low computational effort. An equivalent electrical network could be coupled to the circuit to account for the dynamic heat propagation.

The impact of relevant device and circuit parameters variability on parallel connected SiC MOSFETs has been evaluated by statistical means. This analysis laid the foundations for the development of a guideline for the identification of allowable parameters spread ensuring the safe operation of the parallel array. As a preliminary step, a subset of relevant device and circuit parameters has been identified. With reference to the device, these are the threshold voltage, the current factor, and the MOSFET capacitances; while, with reference to the circuit, the gate resistance and the source stray

inductance have been selected. Successively, the fluctuations of both threshold voltage and current factor have been quantified starting from the static characterization of a set of 20 - 1.2 kV, 36 A SiC power MOSFETs. The resulting experimental values have been found to be normally distributed. The remaining parameters have been assumed to be normally distributed with relative 3σ-spreads of 50% around their mean values. Afterward, the ET simulation of a 200 kHz synchronous stepdown converter based on eight mismatched MOSFETs in terms of V_{TH} and K has been performed. After an operation time of 0.2 s, a significant temperature difference (44.5 ◦C) has been observed between the MOSFETs with the highest and lowest V_{TH} values. Subsequently, the expected turn-off drain over current and the dissipated switching energies have been estimated by running several MC campaigns (each comprising 1200 simulations) on a DPT circuit containing four parallel MOSFETs. Furthermore, the general idea for a procedure to relate the parameters spread to the possible temperature imbalance has been illustrated. Such a procedure is based on the execution of multiple MC ET simulations and on the approximation of the thermal problem to a 1-D equivalent. An example of how its outcomes can be used as a first-order decision rule for the selection of appropriate performance variation limits of parallel SiC MOSFETs has eventually been presented.

Study on fast recovery epitaxial Si diodes (in collaboration w/ Vishay Semiconductor Italia)

The market pushes towards power semiconductor devices with increasingly good performance in terms of efficiency and reliability to be used in a variety of applications. This trend brings the need for more and more stringent requirements of the family of power devices. The design validation of a power diode with a high switching frequency (hereafter referred to as Fast Recovery Epitaxial Diode -FRED-), requires a high ruggedness to avalanche operating conditions. Such characteristic is typically evaluated by the Unclamped Inductive Switching (UIS) test, through which the maximum energy that the devices can withstand during avalanche operation is measured.
The avalanche performance strongly depends on the design of the termination region of the power chip. Such a region is necessary to reduce the gradient of the electric field in boundary region of the main pn junction, which otherwise would have a breakdown voltage (BV) significantly lower than that of the active region.
The use of specific structures for the realization of the termination allows to reach a BV value of the termination region close to the value of the active area.
Nevertheless, during the off-state, the current usually flows through the termination region due to the slightly lower BV of such a region. In addition to that, the corner sections of the termination have an even smaller BV value because of the curvature of the doping profile.
Ideally, the BV of the termination could approximately reach a value very close to that of the active region if a large section of the DIE was dedicated to the termination itself (a possibility might be the adoption of the floating field ring -FFR- termination technology implemented using a large number of floating rings). However, this solution cannot be pursued in reality due to the consequent increase of the DIE cost.
As a result, a study aimed at the identification of the correct balance between the area occupation of the termination and the DIE cost is necessary. The main objective of this activity is to develop an innovative termination exploiting the Junction Termination Extension (JTE) by means of TCAD semiconductor simulations. The peculiarity of the JTE solution is to yield a BV comparable to that given by the FFR technique but with a significantly lower area occupation.

Gate leakage current sensing for *in situ* temperature monitoring of p-GaN gate HEMTs

Gallium Nitride high electron mobility transistors (GaN HEMTs) enable more efficient and compact converters by providing faster switching transients and higher power density than conventional Si power devices. These aspects exacerbate severe electrothermal conditions within the device. Consequently, an online monitoring of the device self-heating is of uttermost importance to improve the thermal management, detect harsh operating conditions (e.g., short circuit and avalanche operation) and evaluate important performance and reliability indicators, such as the converter efficiency or the useful lifetime. Normally-off p-GaN HEMTs have shown a very fast electrothermal response, thus making slow temperature probes ill-suited to grasp the thermal transients. The approaches reported in literature for normally-off p-GaN gate HEMTs are based either on

monolithically integrated sensing elements, or on temperature-sensitive electrical parameters, such as channel resistance (Rch) or gate leakage current (IG,LEAK). However, the solution proposed in literature was verified only on test structures and might not be applicable to commercial devices. Furthermore, no circuit schemes were proposed to apply the temperature sensing strategy during realistic circuit operation of the device. On the other hand, the possibility of using IG,LEAK as a temperature sensitive electrical parameter was adopted in a literature example for normally-on GaN HEMTs, where IG,LEAK is considerably higher than that of the currently available normally-off GaN HEMTs. In a literature example, IG,LEAK is measured as the voltage drop on a gate shunt resistor of 100 Ω, which is a value incompatible with applications requiring a switching frequency in the MHz range. Another method for measuring IG,LEAK was proposed, however, this required a complex ASIC and accurate synchronization to minimize the impact on the regular gate driving. Consequently, the aforementioned challenges related to custom device design or applicability of conventional gate driving circuits make this an open issue. In this paper, we present an effective, yet simple, methodology for the temperature monitoring of voltage-driven p-GaN HEMTs based on IG,LEAK sensing. The proposed solution has been verified by SPICE electrothermal simulations and experiments on commercial devices within and out of safe operating area (SOA).
First, it has been experimentally verified on a commercial device that the gate leakage current shows a remarkable dependence on the temperature and on the gate bias. Such a dependence has been tested during both static and short circuit operation. Afterwards, it has been explored the possibility of using the voltage drop across a diode on the turn-on branch of the gate driver as a parameter equivalent to the gate leakage current. Furthermore, a simple yet effective circuit to sense and amplify the diode voltage drop has also been designed. The applicability of the circuit has been tested during the operation of the DUT in a 1 MHz boost converter investigated by SPICE electrothermal simulation. The circuit does not bring an additional design burden and, once prototyped, its adoption will be further investigated by a thorough experimental campaign by also considering the influence of the device degradation on IG,LEAK.

4. Products

    1. M. Riccio, A. Borghese, L. Maresca, G. Breglio and A. Irace, "Fully-Coupled Electrothermal Simulation of Wide-Area Reverse Conducting IGBTs," 2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Lecco, Italy, 2019, pp. 1-4, doi: 10.1109/THERMINIC.2019.8923497.
    2. A. Borghese, et al., "Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs," Microelectronics Reliability, Volume 114, 2020, 113762, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2020.113762.
    3. A. Borghese, et al., "Statistical Electrothermal Simulation for Lifetime Prediction of Parallel SiC MOSFETs and Modules," 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Cagliari, Italy, 2020, pp. 383-386, doi: 10.1109/IESES45645.2020.9210690.
    4. F. Richardeau et al., "SiC MOSFETs soft and hard failure modes: functional analysis and structural characterization," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020, pp. 170-173, doi: 10.1109/ISPSD46842.2020.9170094.
    5. A. Castellazzi et al., "Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode," Microelectronics Reliability, Volume 114, 2020, 113943, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2020.113943.
    6. [Book chapter] L.Maresca et al., “SiC MOSFETs”, in “Power Electronic devices: physics, applications, failure mechanisms and reliability”, F. Iannuzzo, IET.
    7. [Book chapter in preparation] M. Riccio et al., “Optimum module design I: device modeling and extrinsic parameter spread”, in “SiC power module design and assembly: building in performance, robustness and reliability”, A. Castellazzi, A. Irace, IET.

5. Conferences and Seminars
    - Neapolis Innovation – Technology Day 2020, ST-Microelectronics, Naples, 18/11/2020 →1 poster presentation

- 2020 IEEE 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Caglieri, 2020
  → 1 oral presentation.
- 2020 IEEE 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020.
  → 1 paper, 1 poster presentation.
- 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), Athens, Greece, 2020.
  → 2 papers, 1 oral presentation.

6. Tutorship
   - Co-supervision of BSc student (Luigi Antuono) thesis on “Tecniche di Clustering per la Classificazione di Power MOSFETs in Carburo di Silicio”.
   - Co-supervision of MSc student (Pio Nicola di Costanzo) thesis on “gate driver circuit for in situ temperature monitoring of normally-off p-GaN gate HEMTs”.
   - Co-supervision of MSc student (Domenico Russo) thesis (in progress).