PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Alessandro Borghese

XXXIV Cycle

Training and Research Activities Report – First Year

Tutor: Prof. Andrea Irace

1. Information

Alessandro Borghese received his BSc and MSc degrees in electronic engineering from the University of Naples Federico II. On October 23rd, 2017, he defended a master thesis entitled "Efficiency Estimation and Comparison of Two Inverters for Electric Vehicles: Si vs. SiC Power Devices". The thesis activity was developed as a part of a one-year internship at the Technical Centre of Toyota Motor Europe (Hoge Wei 33, B-1930 Zaventem, Belgium).
After his graduation, Mr. Borghese worked at the Electrothermal Characterization Laboratory (Dept. of Electrical Engineering and Information Technology - Building 2 -, University of Naples Federico II, Via Claudio 21, Naples) from November 2017 to October 2018.
On October 2018, Mr. Borghese took part in the public admission procedure for enrolling at the Information Technology and Electrical Engineering PhD of the University of Naples Federico II. He was awarded with a ministerial scholarship and officially started the 34th PhD cycle on November 1st under the tutorship of Prof. Andrea Irace.
Mr Borghese's research activity is focused on power electronics and it specifically concerns the study of wide bandgap power semiconductor devices.

2. Study and Training activities

During the first year, Alessandro Borghese attended several courses and seminars to expand his knowledge in different areas. A full list of the training activities undertaken by Mr. Borghese is reported below:

- Courses
  - "How to publish a scientific paper" - Aliaksandr Birukou and Elisa Magistrelli – 26/11/2018 (0.4 ECTS)
  - "Elettromagnetismo e Relatività" – Prof. Amedeo Capozzoli – 28/11/2018 to 30/01/2019 (5 ECTS).
  - "Machine Learning" – Prof. Carlo Sansone, et. al. – 05/2019 (3.2 ECTS).
- Seminars
  - "IEEExplore Training and Authorship Workshop", Eszter Lukàcs, 04/04/2019 (0.5 ECTS).
  - "Robots in Medical Applications: An Overview of the Current Medical Robotics from the Industry's Point of View", Vincenzo Schettino, 30/04/2019 (0.6 ECTS).
  - "Medical Thermal Therapy and Monitoring Using Microwave Inverse Scattering", Prof. Antonio Iodice, 02/05/2019 (0.2 ECTS).
  - "Technology Foresight for the Armed Forces: a Structured Journey between Science-Fiction and Reality", Dr. Angela Sara Cacciapuoti and Dr. Marcello Caleffi, 30/05/2019 (0.2 ECTS).
  - "Distributed Radio Systems, Virtual Ran and the Path to 5G", Prof. Amedeo Capozzoli, 30/05/2019 (0.4 ECTS).
  - "How to Turbo Boost your PhD", Prof. Antigone Marino (Dept. of physics, University of Naples Federico II), 05 - 06/2019 (4 ECTS).
- External courses
  - "20th European PhD School Power Electronics, Electrical Machines, Energy Control and Power Systems", Gaeta (Italy) – Prof. Giuseppe Tomasso (University of Cassino), – 20 - 24/05/2019 (4 ECTS). http://www.magento-expert.it/phdschool/
  - "SIE PhD School: Electronics Around the Earth" – Prof. Paolo Colantonio (University of Rome Torvergata) – 24 - 26/06/2019 (4 ECTS). http://sie-2019.uniroma2.it/phd-school/
  - "Summer School on Wide-Bandgap Nitride Devices", Ghent (Belgium) – Dr. Filip Geenen (Ghent University), – 8 - 11/07/2019 (5 ECTS). http://www.inrel-npower.eu/SummerSchool2019

Student: Alessandro Borghese									Tutor: Andrea Irace								Cycle XXXIV									
alessandro.borghese@unina.it									andrea.irace@unina.it																	
	Credits year 1								Credits year 2								Credits year 3									
		1	2	3	4	5	6			1	2	3	4	5	6			1	2	3	4	5	6			
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary	Total	Check
Modules	20	0.4	5		11	5		22	10							0	0							0	22	30-70
Seminars	5			1.1	4.8			5.9	6							0	0							0	5.9	10-30
Research	35	9.6	5	8.9	0	5	10	39	45							0	60							0	39	80-140
	60	10	10	10	16	10	10	66	61	0	0	0	0	0	0	0	60	0	0	0	0	0	0	0	66	180

3. Research activity

Introduction

Mr Borghese's research activity falls in the field of power electronics and, specifically, it focuses on the study of wide bandgap (WBG) power semiconductor devices.

The field of power electronics focuses on the use of solid-state electronic devices for the conversion, control, and processing of electricity and electric power. Silicon (Si) semiconductors have traditionally been employed in fabricating these power circuits. However, as devices and equipment evolve and become more powerful, existing Si power electronics are losing the ability to keep pace with increasing performance demands. This is primarily attributed to the fact that traditional Si device technology has matured to a point where it is pushing the fundamental limitations of this material system. Wide bandgap (WBG) semiconductors have shown the capability to meet the higher performance demands of the evolving power equipment, operating at higher voltages and temperatures and enabling switching frequencies with greater efficiencies compared with existing Si devices. Along with performance improvements, WBG-based power electronics can be fabricated with a much smaller footprint (reduced volume) compared with comparable Si devices due to decreased cooling requirements and smaller passive components, contributing to overall lower system costs.

WBG semiconductors are materials (elements or compounds) whose bandgap (energy difference between valence and conduction bands) is bigger than 1.12 eV, which is the silicon (Si) bandgap value. Two major WBG materials with the potential to enable significant advances in power electronics are silicon carbide (SiC) and gallium nitride (GaN). While SiC currently has limited use in power electronics, its role is expected to grow as it becomes the prevailing WBG replacement for Si in applications requiring device ratings in excess of 600 volts. A major challenge to widespread adoption of SiC power electronics devices is the high cost of substrates and epitaxial materials. These high costs are tied to small production volumes and high manufacturing costs. Significant markets are expected for SiC devices in hybrid and electric vehicles as well as solar inverters and power supplies. SiC diodes are already used with companion Si transistors in photovoltaic (PV) inverters and hybrid vehicle chargers. Their greatest revenue-generating applications are expected to be in industrial motor drives and hybrid and electric vehicles.

GaN is currently widely used in LEDs and radio frequency (RF) amplifiers, and its emergence in power electronics is relatively recent. Challenges for GaN-on-Si semiconductors, the current most cost-effective method for fabricating GaN power devices, are mostly related to their lack of maturity. Issues include overcoming material challenges, such as the high lattice strain at the GaN and Si interface owing to mismatches in the coefficient of thermal expansion. GaN high-electron-mobility transistors (HEMTs) are expected to be the dominant WBG semiconductor replacement for Si in applications requiring device ratings less than 600 V.

Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs

The quantity of applications and pilot projects employing silicon carbide (SiC) MOSFETs as a replacement for conventional silicon (Si) power devices increased over the last two decades. Such a growing diffusion is strongly related to the increasing commercial availability of SiC devices with outstanding static and dynamic performances, which have a direct beneficial impact on the size and the efficiency of the final system. Despite these good characteristics, the current capability of single-

die SiC MOSFETs is typically limited to few hundred Amps, which makes them incompatible with those sectors where high power levels are required. Therefore, in order to exploit the superior properties of such devices in a broader range of possible fields, there is a great interest in paralleling several transistors to reach a desired current rating. Whether the parallelization is achieved at module level (i.e., by connecting together various chips within the same package) or at circuit level (i.e., by wiring a number of discrete devices on the same circuit board), some challenges have to be taken into account during the implementation. In particular, inhomogeneities among inherent device properties, namely on-state resistance RON, threshold voltage VTH, transconductance, breakdown-voltage VBR, as well as assembly-related electrothermal (ET) and electromagnetic mismatches can lead to non-uniform static and dynamic performances. Furthermore, the performance spread may vary over time as the parameters shift with the temperature. As a consequence, some devices might endure an overstress undermining the lifetime or the reliability of the whole assembly. Therefore, developing design guidelines and derating rules is essential for the optimization of parallel configurations of SiC MOSFETs. In order to do so, an indispensable in-depth comprehension of the influence of the parameters spread on the performances of the devices must first be achieved.
Despite the number publications discussing balancing methods and derating rules, none of them is based on a statistical derivation. The latter is of paramount importance, especially when selecting safety margins, as worst-case assumptions tend to overestimate the derating factors. Since SiC devices are still expensive when compared to equally rated Si devices, it is of great interest to minimize the derating requirements. Therefore, the statistical description of parameters variability has been used to extensively analyze ET imbalances of four parallel SiC MOSFETs under inductive load switching and to develop a methodology for deriving a design guideline for the safe operation of parallel SiC devices. The selected key quantities on which this study focuses on are both devices parameters - MOSFET current factor (K), threshold voltage (VTH) and MOSFET capacitances (CGS, CGD and CDS) - and circuit parameters - gate resistance (RGP) and source inductance (LSP).
As a preliminary step, the fluctuations of both threshold voltage and current factor have been quantified starting from the static characterization of a set of 20 - 1.2 kV, 36 A - SiC power MOSFETs. The resulting experimental values have been found to be normally distributed. The remaining parameters have been assumed to be normally distributed with relative 3σ-spreads of 50% around their mean values. Afterwards, the ET simulation of a 200 kHz synchronous step-down converter based on eight mismatched MOSFETs in terms of VTH and K has been performed. After an operation time of 0.2 s, a significant temperature difference (44.5 °C) has been observed between the MOSFETs with the highest and lowest VTH values. Subsequently, the expected turn-off drain over current and the dissipated switching energies have been estimated by running several Monte Carlo (MC) campaigns (each comprising 1200 simulations) on a DPT circuit containing four parallel MOSFETs. Furthermore, the general idea for a procedure to relate the parameters spread to the possible temperature imbalance has been illustrated. Such a procedure is based on the execution of multiple MC ET simulations and on the approximation of the thermal problem to a 1-D equivalent. An example of how its outcomes can be used as a first-order decision rule for the selection of appropriate performance variation limits of parallel SiC MOSFETs has eventually been presented.
After the statistical characterization of the device parameters, the ET behavior of a DC/DC converter containing mismatched parallel SiC MOSFETs has been simulated. Successively, several sets of Monte Carlo (MC) simulations have been conducted. These aimed at statistically quantifying the influence of the selected parameters on the performance spread. Afterwards, the numerical outcomes of such sets of simulations have been used to elaborate a guideline for the safe long-term operation of parallel SiC MOSFETs.

Study on fast recovery epitaxial Si diodes (in collaboration w/ Vishay Semiconductor Italia)

The market pushes towards power semiconductor devices with increasingly good performance in terms of efficiency and reliability to be used in a variety of applications. This trend brings the need for more and more stringent requirements of the family of power devices. The design validation of a power diode with a high switching frequency (hereafter referred to as Fast Recovery Epitaxial Diode -FRED-), requires a high ruggedness to avalanche operating conditions. Such characteristic is

typically evaluated by the Unclamped Inductive Switching (UIS) test, through which the maximum energy that the devices can withstand during avalanche operation is measured.
The avalanche performance strongly depends on the design of the termination region of the power chip. Such a region is necessary to reduce the gradient of the electric field in boundary region of the main pn junction, which otherwise would have a breakdown voltage (BV) significantly lower than that of the active region.
The use of specific structures for the realization of the termination allows to reach a BV value of the termination region close to the value of the active area.
Nevertheless, during the off-state, the current usually flows through the termination region due to the slightly lower BV of such a region. In addition to that, the corner sections of the termination have an even smaller BV value because of the curvature of the doping profile.
Ideally, the BV of the termination could approximately reach a value very close to that of the active region if a large section of the DIE was dedicated to the termination itself (a possibility might be the adoption of the floating field ring -FFR- termination technology implemented using a large number of floating rings). However, this solution cannot be pursued in reality due to the consequent increase of the DIE cost.
As a result, a study aimed at the identification of the correct balance between the area occupation of the termination and the DIE cost is necessary. The main objective of this activity is to develop an innovative termination exploiting the Junction Termination Extension (JTE) by means of TCAD semiconductor simulations. The peculiarity of the JTE solution is to yield a BV comparable to that given by the FFR technique but with a significantly lower area occupation.

4. Products

1. A. Borghese et al., "Effect of Parameters Variability on the Performance of SiC MOSFET Modules," 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Nottingham, 2018, pp. 1-5. doi: 10.1109/ESARS-ITEC.2018.8607593
2. M. Riccio et al., "Experimental analysis of electro-thermal interaction in normally-off pGaN HEMT devices," 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Nottingham, 2018, pp. 1-6. doi: 10.1109/ESARS-ITEC.2018.8607347
3. A. Borghese et al., "Statistical Analysis of the Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1527-1538, Sept. 2019. doi: 10.1109/JESTPE.2019.2924735
4. A. Borghese et al., "An Experimentally Verified 3.3 kV SiC MOSFET Model Suitable for High-Current Modules Design," 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 2019, pp. 215-218. doi: 10.1109/ISPSD.2019.8757576
5. A. Borghese et al., “An Efficient Simulation Methodology to Quantify the Impact of Parameter Fluctuations on the Electrothermal Behavior of Multichip SiC Power Modules,” in Silicon Carbide and Related Materials 2018, 2019, vol. 963, pp. 855–858.
6. M. Riccio et al., "Fully-Coupled Electrothermal Simulation of Wide-Area Reverse Conducting IGBTs," 2019 IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Lecco, 2019
7. A. Fayyaz et al., "Aging and failure mechanisms of SiC Power MOSFETs under repetitive shortcircuit pulses of different duration," 2019 International Conference on Silicon Carbide and Related Materials (ICSCRM), Kyoto, 2019
8. [Book chapter in preparation] L.Maresca et al., “SiC MOSFETs”, in “Power Electronic devices: physics, applications, failure mechanisms and reliability”, F. Iannuzzo, IET.

5. Conferences and Seminars
   - Neapolis Innovation – Technology Day 2018, ST-Microelectronics, Naples, 21/11/2018

→1 poster presentation

- 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Nottingham, 2018
  →2 papers, 1 oral presentation.
- 2019 Meeting Annuale Società Italiana di Elettronica (SIE), Rome, 2019.
  → 1 paper, 1 oral presentation.
- 20th European PhD School Power Electronics, Electrical Machines, Energy Control and Power Systems", Gaeta (Italy) – Prof. Giuseppe Tomasso (University of Cassino), – 20 - 24/05/2019
  → 1 poster presentation.
- Summer School on Wide-Bandgap Nitride Devices", Ghent (Belgium) – Dr. Filip Geenen (Ghent University), – 8 - 11/07/2019
  → 1 poster presentation.
- Seminar entitled "Fundamentals of Pulse Oximetry" held at "CI-LAM Summer school 1st edition", University of Naples Federico II, 15 – 28/07/2019.

6. Activity abroad

   - 25.02.2019-29.03.2019, University of Nottingham, Power Electronics, Machines and control Group (Prof. Alberto Castellazzi), UK.
     Study on failure mechanisms of SiC MOSFETs during short circuit events (University of Nottingham, PEMC group, Prof. Alberto Castellazzi).

7. Tutorship
   - Co-supervision of BSc student (Salvio Paciello) thesis on "Electrical Characterization of GaN HEMTs".
   - Co-supervision of BSc student (Pierluigi Sozio) thesis on "Pulsed Curve-Tracer for Power Devices".
   - Co-supervision of BSc student (Giuliano Mattiello) thesis on "Pulsed Curve-Tracer for Power Devices".
   - Co-tutor of lab sessions at "CI-LAM Summer school 1st edition", University of Naples Federico II, 15 – 28/07/2019.