Year-End Presentation

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DIETI UNIVERSITA' DEGLI STUDI DI NAPOLI FEDERICO II
DIPARTIMENTO DI INGEGNERIA ELETTRICA E DELLE TECNOLOGIE DELL'INFORMAZIONE

Outline

My background

- Master Degree in Information Technology at University of Naples - Federico II
- Master Thesis: *Un prototipo di middleware configurabile – nel dominio ferroviario – per fault detection e comunicazione affidabile*;
  - This thesis work is part of a joint project involving the DIETI and Rete Ferroviaria Italiana - RFI - Gruppo delle ferrovie dello Stato S.p.a.;
- Currently involved in three research projects:
  - The railway domain;
  - Approximate Computing;
  - Hardware security;

Approximate Computing

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- The size of the data to be processed by computer systems is rapidly growing.
- Unmatched technology progress.
  - CMOS technology is approaching its physical limit.
  - Die-shrinking is not a viable solution anymore.
- Energy consumption is an emerging issue.
- Many applications show error resiliency.
  - Noisy input data.
  - Redundant computations.
  - Self-healing.
- Error resiliency is exploited by Approximate Computing.
- Relaxing accuracy requirements to achieve some desired properties.
  - Typically, energy efficiency.

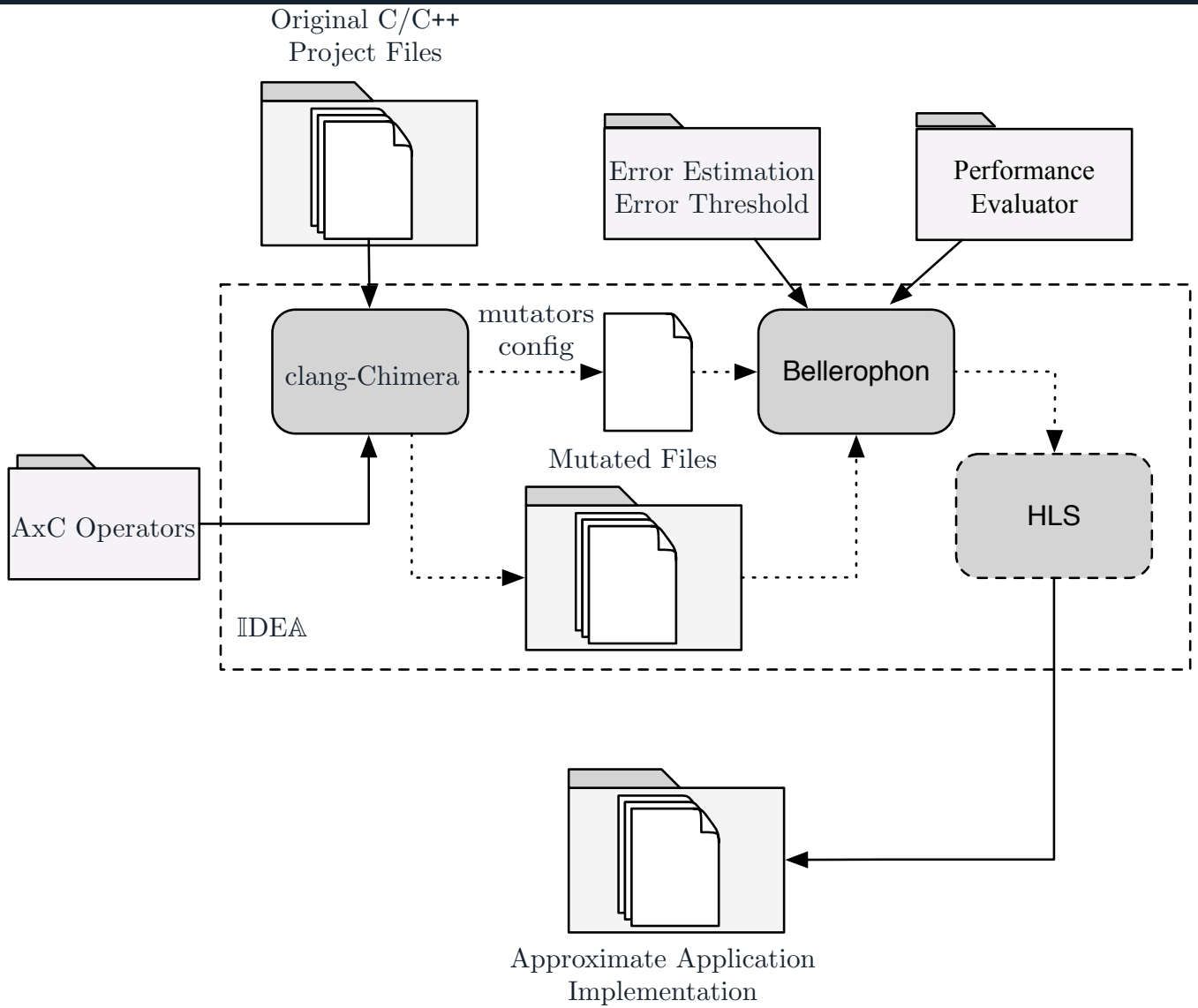
Challenges

- Naive approaches, such as uniform approximation, is unlikely to be efficient.
- Many techniques have been proposed.
  - Too tied with a specific application.
  - **None of them have general applicability**.
- Output monitoring is mandatory.
  - Application requirement must be met.
  - Induced error must fall below an user-defined/application-dependent threshold.
- Different approximate versions of the same application have to be evaluated (quickly).
  - **There is no generic automation tool**.

The IDEA framework

- Clang-Chimera
  - It is a source-to-source *mutation engine*.
  - It Needs a C/C++ model of the algorithm to be approximated.
  - It is based on Clang-LLVM.
  - It applies used-defined mutations on the Abstract Syntax Tree (AST)
- Bellerophon
  - It is a design-space exploration tool designed to solve Multi-objective Optimization Problems (MOPs).
  - It is based on Non-dominated Sorted Genetic Algorithm (NSGA)-II.
  - It exploits the Clang-LLVM Just-In-Time (JIT) compiler.
  - The evaluation is based on three fitness functions:
    - *error function*: expresses the measured amount of error, w.r.t. a reference solution;
    - *reward function*: rewards certain characteristics of one solution;
    - *penalty function*: penalizes infeasible solutions w.r.t. the degrees of constraint.

The IDEA Work-flow



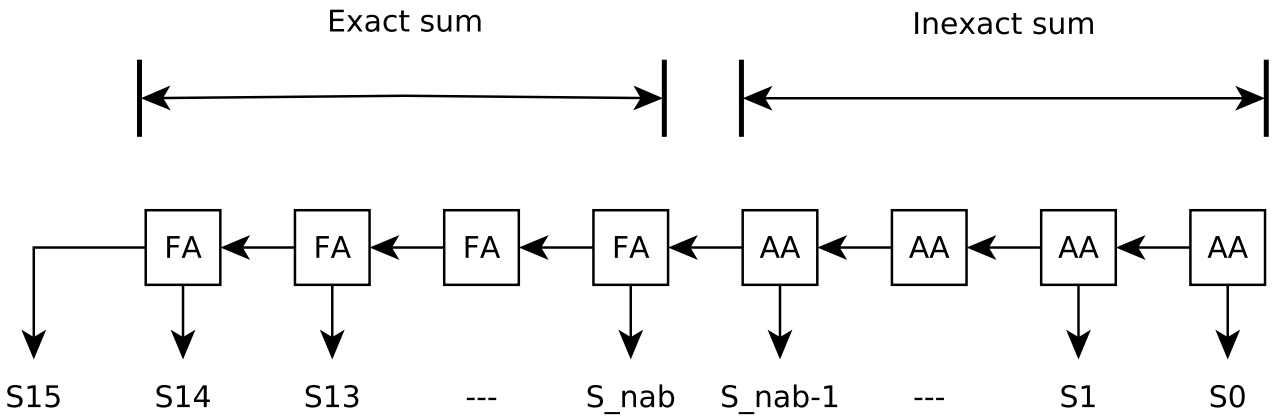
The DCT: a case study (1/2)

Approximate DCT

- A configurable, approximate DCT HW-accelerator is implemented.
  - Image-processing is one of the best field of application for AxC.
  - The DCT is the most demanding step of the JPEG compression algorithm.
- Many fast-algorithms have been proposed.
  - No need for floating-point operations.
  - No need for multiplications.
  - **Only integer additions**.
- **To further reduce area and energy requirements, inexact adders can be adopted**.

The DCT: a case study (2/2)

Approximate DCT



- 7 different DCT-computation algorithms have been tested.
- 10 different inexact adder cells have been considered.
- Source of approximation:
  - The Number of Approximated Bits (NABs) of the sum.
  - The type of cells.
- Synthesised on Xilinx Zynq-7010 FPGA and 65nm CMOS ASIC.

Experimental Results (1/2)

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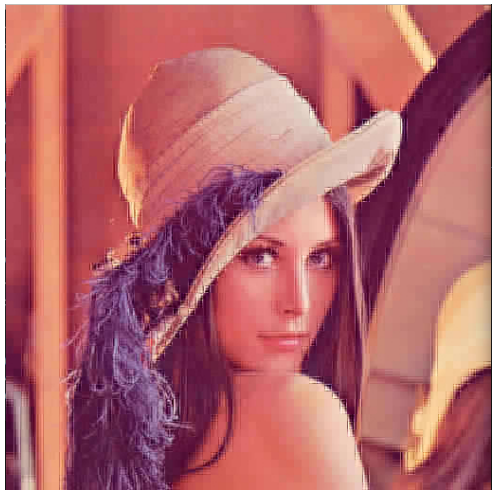
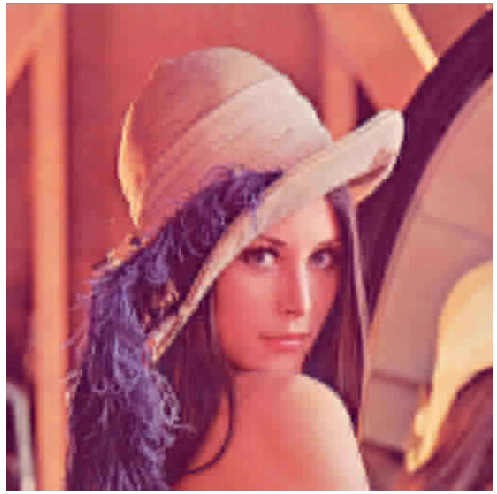
Original Image

BAS-08 with approximation

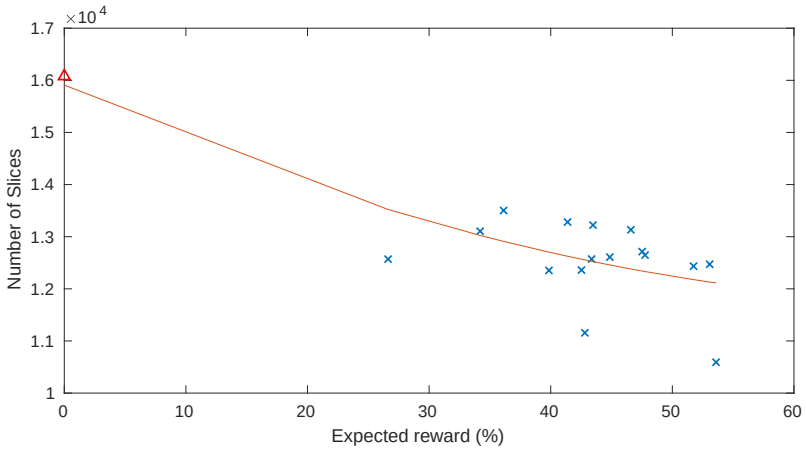


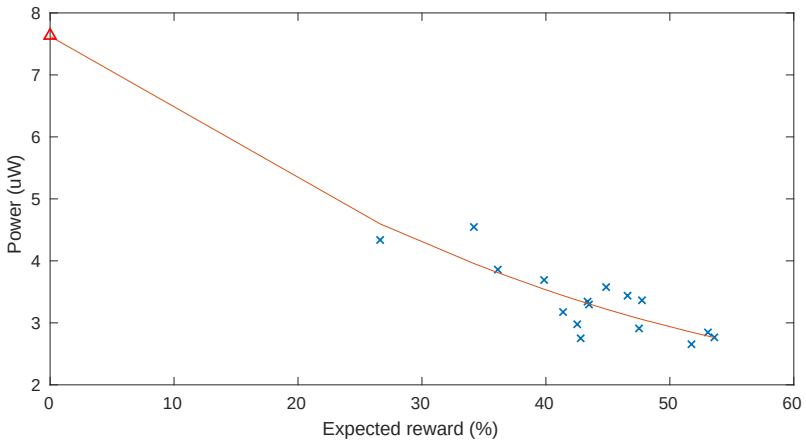
BAS-08 with 33% error, 22% reward



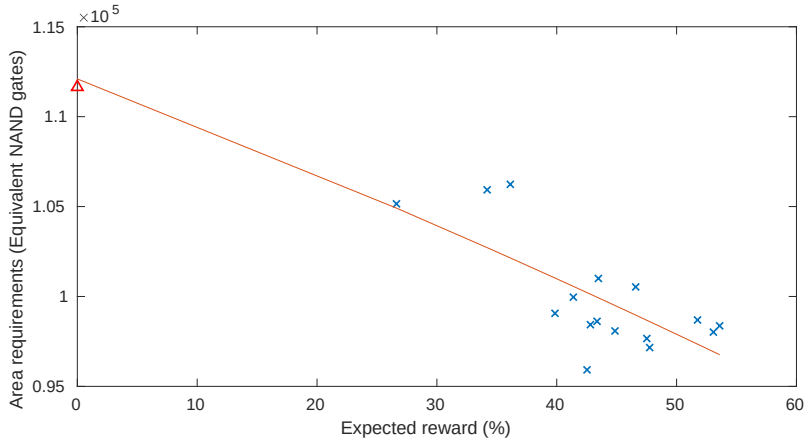
Experimental Results (2/2)

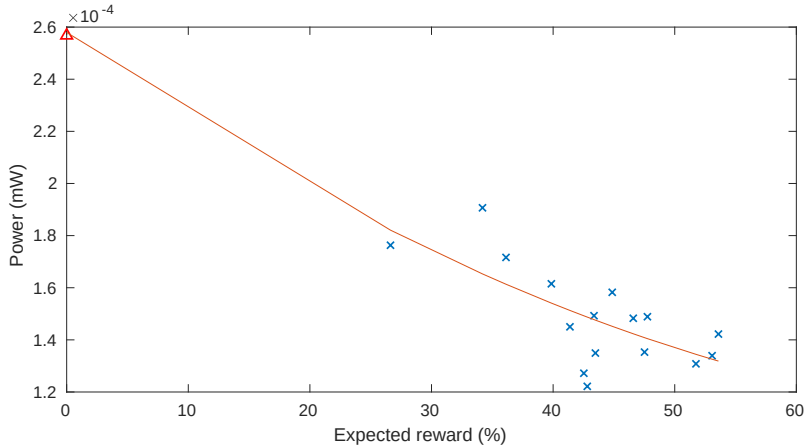
FPGA





ASIC





Publications

Title:	Approximate Computing by Mutation: a General Approach
Type:	Journal article
Publisher:	IEEE Transaction on Computers
Status:	Under Review
Title:	Advancing Synthesis of Decision Tree Based Multiple Classifier Systems: an Approximate Computing Case Study
Type:	Journal article
Status:	Still writing

Future works

- Apply the same methodology in different fields of application.
  - Machine-learning and classifiers.
- Hardware is typically designed using Hardware Description Languages (HDLs) such as VHDL or Verilog.
- The need of a C/C++ model is a limitation.
  - The mutated C/C++ source code must be used to re-implement the algorithm.
  - GHDL-Chimera: a VHDL source-to-source mutation engine.

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