PhD in Information Technology and Electrical Engineering

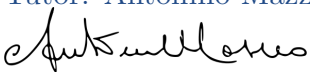
Università degli Studi di Napoli Federico II

PhD Student: Salvatore Barone

XXIX Cycle

Training and Research Activities Report – Third Year

Tutor: Antonino Mazzeo



1 Study and Training activities

This section lists all the courses and seminars I have attended during the last year. The list does not follow a chronological order.

Courses

Title: Data Management
Date: 08/02/2021
Lecturer: Flora Amato
Credits: 6

Title: IEEE/DEI Summer Ph.D. School of Information Engineering "Silvano Pupolin" – SSIE 2021
Date: July 12 – 16, 2021
Lecturer: various
Credits: 5

Seminars

Title: Robot Manipulation and Control
Date: 17/11/2020
Lecturer: Prof. Bruno Siciliano
Credits: 0.5

Title: Beyond Einstein Gravity: Dark Energy and Dark Matter as Curvature Effects
Date: 19/11/2020
Lecturer: Salvatore Capozziello
Credits: 0.3

Title: The Ohta-Kawasaki model for diblock copolymers: stability and minimality of critical points
Date: 26/11/2020
Lecturer: Prof. Nicola Fusco
Credits: 0.3

Title: Network Systems, Kuramoto Oscillators, and Synchronous Power Flow
Date: 3/12/2020
Lecturer: Francesco Bullo
Credits: 0.3

Title: Force and Visual Control for Safe Human-Robot Interaction
Date: 3/12/2020
Lecturer: Prof. Bruno Siciliano
Credits: 0.4

Title: Measuring the expansion of the universe with quasars
Date: 10/12/2020
Lecturer: Prof. Guido Risaliti
Credits: 0.3

Title: Probing gravitational field: a fundamental viewpoint
Date: 21/01/20201
Lecturer: Prof. Lorenzo Fatibene
Credits: 0.3

Title: Quantum Simulators
Date: 28/01/2021
Lecturer: Prof. Rosario Fazio

Title: Engineering the firearm ecosystem: research on media coverage and firearm acquisition in the aftermath of a mass shooting
Date: 04/02/2021
Lecturer: Prof. Maurizio Porfiri
Credits: 0.3

Title: Measuring the cosmological parameters with SNe-Ia and Gamma-ray Bursts
Date: 11/02/2021
Lecturer: Prof. Maurizio Porfiri
Credits: 0.3

Title: Designing a Socially Assistive Robot for adaptive and personalized assistance to patients with dementia.
Date: 17/02/2021
Lecturer: Dr. Antonio Andriella
Credits: 0.2

Title: Variational approximations of the Griffith functional
Date: 19/02/2021
Lecturer: Prof. Francesco Solombrino
Credits: 0.3

Title: Astroparticle Physics in the Era of Multi-messenger Astronomy
Date: 04/03/2021
Lecturer: Prof. Gennaro Miele

Title: The coming revolution of Data driven Discovery (a fourth Methodological Paradigm of Science)
Date: 25/03/2021
Lecturer: Dr. Giuseppe Longo
Credits: 0.3

Title: Classical Cepheids as distance indicators.

Date: 15/04/2021
Lecturer: Prof.ssa Marcella Marconi
Credits: 0.3

Title: Dark Energy and Cosmic Acceleration
Date: 13/05/2021
Lecturer: Prof.Jailson Alcaniz
Credits: 0.3

Title: Synchronization in complex networks, hypergraphs and simplicial complexes
Date: 27/05/2021
Lecturer: Dr. Stefano Boccaletti
Credits: 0.3

Title: Dynamics of PDEs and recurrent motions
Date: 03/06/2021
Lecturer: Dr. Pietro Baldi
Credits: 0.3

Title: What Is Matter According to Particle Physics, and Why Try to Observe Its Creation in a Lab?
Date: 15/07/2021
Lecturer: Prof. Francesco Vissani
Credits: 0.3

2 Research activities

Currently, my research activity focuses on three main themes: approximate computing, which is my main topic, safety-critical railway applications and hardware-security and trust. In the following, they will be discussed in detail.

Approximate Computing Concerning this field, my research activity focuses on applying Approximate Computing techniques to predictive models, such as random-forest classifiers or neural networks. So far, multiple classifier systems and neural networks have been increasingly designed to take advantage of hardware features, such as high parallelism and computational power. Indeed, compared to software implementations, hardware accelerators guarantee higher throughput and lower latency. Nevertheless, the required silicon area makes the design of a hardware accelerator unfeasible, hindering the adoption of commercial configurable devices. Anyway, by exploits the gap between the high accuracy level provided by a computer system and the moderate accuracy required by a given application, this design paradigm allows achieving performance gains or energy savings.

The railway domain With regard to applications in the railway sector, I am currently involved in the design of a novel architecture for redundant fail-safe safety-critical systems in the railway domain, as part of a joint project involving Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). This research activity is still ongoing, but it has produced several intermediate products. Four thesis works has been completed this year, and two more are still ongoing.

Hardware security and trust My research activity concerns mutual authentication protocols implemented using Physical Unclonable Functions (PUFs). In particular, the implementation of a protocol to allow sensor nodes of a wireless sensors network to authenticate themselves while communicating. This year, one thesis work has been completed on this topic.

3 Products

In this section are listed all the works I have written - or am still writing - during the last year. The list is organized by research topic and does not follow a chronological order.

Approximate computing

Title: Advancing synthesis of decision tree-based multiple classifier systems: an approximate computing case study
Authors: Mario Barbareschi, Salvatore Barone & Nicola Mazzocca
Type: Journal Article
Abstract: So far, multiple classifier systems have been increasingly designed to take advantage of hardware features, such as high parallelism and computational power. Indeed, compared to software implementations, hardware accelerators guarantee higher throughput and lower latency. Although the combination of multiple classifiers leads to high classification accuracy, the required area overhead makes the design of a hardware accelerator unfeasible, hindering the adoption of commercial configurable devices. For this reason, in this paper, we exploit approximate computing design paradigm to trade hardware area overhead off for classification accuracy. In particular, starting from trained DT models and employing precision-scaling technique, we explore approximate decision tree variants by means of multiple objective optimization problem, demonstrating a significant performance improvement targeting field-programmable gate array devices.
Journal: Knowledge and Information Systems, volume 63, number 6, pages 1577–1596
Publisher: Springer London

Title: Multi-Objective Application-Driven Approximate Design Method
Authors: Salvatore Barone, Marcello Traiola, Mario Barbareschi & Alberto Bosio
Type: Journal Article
Abstract: Approximate Computing (AxC) paradigm aims at designing computing systems that can satisfy the rising performance demands and improve the energy efficiency. AxC exploits the gap between the level of accuracy required by the users, and the actual precision provided by the computing system, for achieving diverse optimizations. Various AxC techniques have been proposed so far in the literature at different abstraction levels from hardware to software. These techniques have been successfully utilized and combined to realize approximate implementations of applications in various domains (e.g. data analytic, scientific computing, multimedia and signal processing, and machine learning). Unfortunately, state-of-the-art approximation methodologies focus on a single abstraction level, such as combining elementary components (e.g., arithmetic operations) which are firstly approximated using component-level metrics and then combined to provide a good trade-off between efficiency and accuracy at the application level. This hinders the possibility for designers to explore different

approximation opportunities, optimized for different applications and implementation targets. Therefore, we designed and implemented E-IDEA, an automatic framework that provides an application-driven approximation approach to find the best approximate versions of a given application targeting different implementations (i.e., hardware and software). E-IDEA compounds 1) a source-to-source manipulation tool and 2) an evolutionary search engine to automatically realize approximate application variants and perform a Design-Space Exploration (DSE). The latter results in a set of non-dominate approximate solutions in terms of trade-off between accuracy and efficiency. Experimental results validate the effectiveness and the flexibility of the approach in generating optimized approximate implementations of different applications, by using different approximation techniques and different accuracy/error metrics and for different implementation targets.

Journal: IEEE Access
Publisher: IEEE

Title: A Catalog-based AIG-Rewriting Approach to theDesign of Approximate Components
Authors: Mario Barbareschi, Salvatore Barone, Nicola Mazzocca, and Alberto Moriconi
Type: Journal Article
Abstract: As computational and energy efficiency of computer systems are becoming increasingly relevant requirements, traditional design paradigms are bound to become no longer appropriate, as they cannot guarantee significant improvements. Approximate Computing (AxC) has been introduced as a potential candidate to achieve better performances, by relaxing non-critical functional specifications. Anyway, several challenges need to be addressed in order to exploit its potential. In this paper, we propose a systematic and application-independent approximate design approach to converge towards a Pareto-front of approximate configurations for digital circuits. Our approach is based on local rewriting of and-inverter graphs, reducing the number of nodes and possibly resulting in lower hardware resources requirements. We adopt multi-objective optimization to carefully introduce approximation while leading to optimal trade-offs between error and savings. We evaluate our approach using different benchmarks, and, in order to measure actual gains, we perform FPGA synthesis of Pareto-optimal approximate configurations. Experimental results show that the proposed approach allows performing a meaningful exploration of the design space to find the best trade-offs in a reasonable time, thus resulting in approximate circuits exhibiting lower requirements and restrained error. Furthermore, our approach allows significant improvements over state-of-the-art works from the scientific literature.
Journal: IEEE
Publisher: IEEE
Note: this manuscript is currently undergoing a second-stage review step.

Title: A Genetic-Algorithm-Based Approach to the Design of DCT Hardware Accelerators
Authors: Mario Barbareschi, Salvatore Barone, Alberto Bosio, Marcello Traiola, Jie Han
Type: Journal Article
Abstract: As modern applications demand an unprecedented level of computational resources, traditional computing system design paradigm sare no longer adequate to guarantee significant performance enhancement at an affordable cost. Approximate Computing (AxC) ha sbeen introduced as a potential candidate to achieve better computational performances by relaxing non-critical functional system specifications. In this paper, we propose a systematic and high-abstraction-level approach allowing the automatic generation of near Pareto-optimal approximate configurations for a Discrete Cosine Transform (DCT) hardware accelerator. We obtain the approximate variants by using approximate operations, having configurable approximation degree, rather than full-precise ones. We use a genetic searching algorithm to find the appropriate tuning of the approximation degree leading to optimal trade-offs between accuracy and gains. Finally, to evaluate the actual HW gains, we synthesize non-dominated approximate DCT variants for two different target technologies, namely Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs). Experimental results show that the proposed approach allows performing a meaningful exploration of the design space to find the best trade-offs ina reasonable time. Indeed, compared to the state-of-the-art work on approximate DCT, the proposed approach allows an 18% average energy improvement while providing at the same time image quality improvement.
Journal: The ACM Journal on Emerging Technologies in Computing Systems
Publisher: ACM
Note: this manuscript is currently undergoing a second-stage review step.

The railway domain

Title: Progettazione agile di applicazioni critiche per il dominio ferroviario
Type: Master Thesis (as Co-rapporteur)
Status: Released

Title: Interrupts handling in MPSoC hard real-time domain system
Type: Master Thesis (as Co-rapporteur)
Status: Released

Title: Metodologie di sviluppo software safety critical per applicazioni ferroviarie
Type: Master Thesis (as Co-rapporteur)
Status: Released

Title: Progettazione model-based di applicazioni ferroviarie safety-critical

Type: Master Thesis (as Co-rapporteur)
Status: Released

Title:: Libreria Interfacce I/O ATO - Definizione dell'architettura
Type:: Software requirements specification
Status:: Released
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:: SCSC - Sistema Controllo e Smistamento delle Comunicazioni
Type:: Software library
Status:: Under development
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:: Manuale d'uso e istallazione della libreria SCSC
Type:: User Manual
Status:: Released
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:: Specifica dei Requisiti Software dello Strato Middleware
Type:: Technical document
Status:: Under development
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which

aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signalling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.

Title:: Design architetturale dello strato Middleware
Type:: Technical document
Status:: Under development
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signaling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.

Title:: MASK - Middleware tra Applicativi Software e Kernel
Type:: Software library
Status:: Under development
Description:: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signalling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.

Title: Scrum for Safety: Agile Development in Safety-critical Software Systems
Authors: Riccardo Carbone, Salvatore Barone, Mario Barbareschi, Valentina Casola
Type: Conference paper
Abstract: The adoption of agile methodologies in all domains of software development is a desired goal. Unfortunately, many obstacles have been meet in the past for a full adoption in secure and safe systems, where different standards and operational constraints apply. In this paper we propose a

novel agile methodology to be applied in the development of safety critical systems. In particular, we developed an extension of the well-known Scrum methodology and discussed the complete workflow. We finally validated the applicability of the methodology over a real case study from the railway domain.

Conference: 14th International Conference on the Quality of Information and Communications Technology - QUATIC 2021

Hardware security and trust

Title: Enforcing mutual authentication and confidentiality in Wireless Sensor Networks using Physically Unclonable Functions: a case study

Authors: Mario Barbareschi, Salvatore Barone, Alfonso Fezza, Erasmo La Montagna

Type: Conference paper

Abstract: The technological progress we witnessed in recent years has led to a pervasive usage of smart and embedded devices in many application domains. The monitoring of Power Delivery Networks (PDNs) is an example: the use of interconnected sensors makes it possible to detect faults and to dynamically adapt the network topology to isolate and compensate for them. In this paper we discuss how Fault-Detection, Isolation and Service Recovery (FDISR) for PDNs can be modeled according to the fog-computing paradigm, which distributes part of the computation among edge nodes and the cloud. In particular, we consider an FDISR application on Medium-Voltage PDNs (MV-PDNs) based on a Wireless Sensor Network (WSN) whose nodes make use of the Long Range (LoRa) technology to communicate with each other. Security concerns and the attack model of such application are discussed, then the use of a communication protocol based on the Physically Unclonable Functions (PUFs) mechanism is proposed to achieve both mutual authentication and confidentiality. Finally, an implementation of the proposal is presented and evaluated w.r.t. security concerns and communication overhead.

Conference: 14th International Conference on the Quality of Information and Communications Technology - QUATIC 2021