PhD in Information Technology and Electrical Engineering

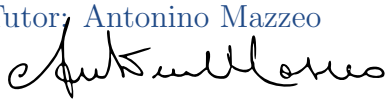
Università degli Studi di Napoli Federico II

PhD Student: Salvatore Barone

XXIX Cycle

Training and Research Activities Report – Second Year

Tutor: Antonino Mazzeo



1 Study and Training activities

This section lists all the courses and seminars I have attended during the last year. The list does not follow a chronological order.

Courses

Title:	Safety Critical Systems for Railway Traffic Management
Lecturer(s):	Mario Barbareschi, Salvatore Barone, Erasmo La Montagna
Credits Earned:	6,6

Title:	Scientific Programming and Visualization with Python
Lecturer(s):	A. Botta
Credits Earned:	3

Title:	Virtualization technologies and their applications
Lecturer(s):	L. De Simone
Credits Earned:	4

Title:	Innovation management, entrepreneurship and intellectual property
Lecturer(s):	P. Rippa
Credits Earned:	5

Title:	Machine Learning
Lecturer(s):	M. Aiello, A. Corazza, D. Gragnaniello, F. Isgrò, R. Prevete, F.Raimondi, C. Sansone
Credits Earned:	4

Seminars

Title:	Lo spazio cibernetico come dominio bellico
Lecturer(s):	Dott. G. P. Siroli
Credits Earned:	0,4

Title:	Introduction to CERN and wakefield measurements at CLEAR
Lecturer(s):	Ing. A. Gilardi
Credits Earned:	0,4

Title:	Marked point process for object detection and tracking in high resolution images: application to remote sensing data
Lecturer(s):	Prof. J. Zerubia
Credits	0,2
Earned:	

Title:	Cybersecurity and fuzzing for robots, blockchain and more
Lecturer(s):	Dr. A. K. Iannillo
Credits	0,2
Earned:	

Title:	Large Scale Training of Deep Neural Networks
Lecturer(s):	Giuseppe Fiameni
Credits	0,5
Earned:	

Title:	Exploring Autonomy in Robotic Flexible Endoscopy
Lecturer(s):	P. Valdastri
Credits	0,4
Earned:	

Title:	Valutazione dei livelli di esposizione e del rispetto dei limiti. Il ruolo delle ARPA / Misure di segnali complessi nell'ambiente: Sistemi 4G / Interconfronto
Lecturer(s):	S. Adda, D. Franci
Credits	1
Earned:	

Title:	Valutazione dei livelli di esposizione e del rispetto dei limiti Antenne e 5G / Misure di segnali complessi nell'ambiente: Sistemi 5G / Estrapolazioni su segnali 4G e 5G
Lecturer(s):	MD Migliore, D. Franci, S. Adda, S. Pavoncelli
Credits	1
Earned:	

2 Research activities

Currently, my research activity focuses on three main themes: approximate computing, which is my main topic, safety-critical railway applications and hardware-security and trust. In the following, they will be discussed in detail.

Approximate Computing Concerning this field, my research activity focuses on applying Approximate Computing techniques to predictive models, such as random-forest classifiers or neural networks. So far, multiple classifier systems and neural networks have been increasingly designed to take advantage of hardware features, such as high parallelism and computational power. Indeed, compared to software implementations, hardware accelerators guarantee higher throughput and lower latency. Nevertheless, the required silicon area makes the design of a hardware accelerator unfeasible, hindering the adoption of commercial configurable devices. Anyway, by exploits the gap between the high accuracy level provided by a computer system and the moderate accuracy required by a given application, this design paradigm allows achieving performance gains or energy savings.

The railway domain With regard to applications in the railway sector, I am currently involved in the design of a novel architecture for redundant fail-safe safety-critical systems in the railway domain, as part of a joint project involving Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). This research activity is still ongoing, but it has produced several intermediate products. Two thesis works has been completed this year, and six more are still ongoing.

Hardware security and trust My research activity concerns mutual authentication protocols implemented using Physical Unclonable Functions (PUFs). In particular, the implementation of a protocol to allow sensor nodes of a wireless sensors network to authenticate themselves while communicating. This year, one thesis work has been completed on this topic.

3 Products

In this section are listed all the works I have written - or am still writing - during the last year. The list is organized by research topic and does not follow a chronological order.

Approximate computing

Title:	Advancing Synthesis of Decision Tree Based Multiple Classifier Systems: an Approximate Computing Case Study
Type:	Journal article
Publisher:	Knowledge and Information Systems (KIAS)
Status:	Under review
Abstract:	So far, multiple classifier systems have been increasingly designed to take advantage of hardware features, such as high parallelism and computational power. Indeed, compared to software implementations, hardware accelerators guarantee higher throughput and lower latency. Although the combination of multiple classifiers leads to high classification accuracy, the required area overhead makes the design of a hardware accelerator unfeasible, hindering the adoption of commercial configurable devices. For this reason, in this paper, we exploit Approximate Computing design paradigm to trade hardware area overhead off for classification accuracy. In particular, starting from trained DT models and employing precision-scaling technique, we explore approximate decision tree variants by means of multiple objective optimization problem, demonstrating a significant performance improvement targeting Field Programmable Gate Array (FPGA) devices.

Title: An Generit-algorithm based approach for the design of Approximate DCT hardware accelerators
Type: Journal article
Publisher: IEEE Transaction on Emerging Topics in Computing
Status: Under review
Abstract: As modern applications demand an unprecedented level of computational resources, traditional computing system design paradigms are no longer adequate to guarantee significant performance enhancement at an affordable cost. Approximate Computing (AxC) has been introduced as a potential candidate to achieve better computational performances by relaxing non-critical functional system specifications. In this paper, we propose a systematic and high-abstraction-level approach allowing the automatic generation of Pareto-optimal approximate configurations for a Discrete Cosine Transform (DCT) hardware accelerator. We obtain the approximate variants by using approximate operations, having configurable approximation degree, rather than full-precise ones. We use a genetic searching algorithm to find the Pareto-optimal tuning of the approximation degree leading to optimal trade-offs between accuracy and gains. Finally, to evaluate the actual HW gains, we synthesize Pareto-optimal approximate DCT variants for two different target technologies, namely Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs). Experimental results show that the proposed approach allows performing a meaningful exploration of the design space to find the best trade-offs in a reasonable time. Indeed, compared to the state-of-the-art work on approximate DCT, the proposed approach allows an 18% average energy improvement while providing at the same time image quality improvement.

Title: Automatic Generation of Application-level Approximate Variants
Type: Journal article
Status: Still writing
Abstract: Approximate Computing paradigm (AxC) aims at designing computing systems that can satisfy the rising performance demands and improve the energy efficiency. AxC exploits the gap between the level of accuracy required by the users and the actual precision provided by the computing system, for achieving diverse optimizations. Various AxC techniques have been proposed so far in the literature, at different abstraction levels, ranging from hardware to software. These techniques have been successfully exploited at application-level in various domains. Examples are data analytics, scientific computing, multimedia and signal processing, and machine learning domains. Unfortunately, a general and systematic methodology to automatically define approximate applications is still an open challenge. More in detail, for a given application, it is not trivial to identify which portion of the application can be approximated and which AxC technique has to be applied. Bearing in mind such a lack of generality, in this paper we introduce a general methodology that allows easily modeling and applying any AxC technique to any application. We designed and implemented IDEAA, an automatic framework that compounds (i) a source-to-source manipulation tool and (ii) an evolutionary search engine, to find the best approximation version of a given application w.r.t. the specific accuracy level required. Experimental results validate its effectiveness in generating optimized approximate applications targeting different implementations (i.e., hardware and software).

Title:	Catalog-based AIG-rewriting Approximate Logic Synthesis Approach for Digital Logic Circuits
Type:	Journal article
Status:	Still writing
Abstract:	With the reaching of the physical limit for the current Complementary Metal-Oxide Semiconductor (CMOS) technology, Scientific research has began shifting its focus to other technological solutions, that, at the time this paper is written, are not yet mature and robust enough to be largely adopted. A promising solution is the Approximate Computing (AxC) design paradigm, which saves area on silicon by relaxing the accuracy constraints of a given application. With the support of automated tools, this paper proposes a methodology that allows designers of combinational logic circuits to define the functional specifications of a circuit and output accuracy constraints in order to obtain approximate versions of a given circuit that meet those constraints and have lower silicon area requirements. Several benchmarks were used to evaluate the methodology, obtaining encouraging results for Field Programmable Gate Array (FPGA) synthesis.

The railway domain

Title:	Cooperazione tra task applicativi di un sistema di segnalamento ferroviario in ambiente safety critical
Type:	Master Thesis (as Co-rapporteur)
Status:	Released

Title:	Realizzazione di un prototipo per il segnalamento ferroviario: sviluppo di un middleware adibito a gestione delle ridondanze e a comunicazioni affidabili
Type:	Master Thesis (as Co-rapporteur)
Status:	Released

Title:	Libreria Interfacce I/O ATO - Definizione dell'architettura
Type:	Software requirements specification
Status:	Under development
Description:	This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:	SCSC - Sistema Controllo e Smistamento delle Comunicazioni
Type:	Software library
Status:	Under development
Description:	This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:	Manuale d'uso e istallazione della libreria SCSC
Type:	User Manual
Status:	Under development
Description:	This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use.

Title:	Specifica dei Requisiti Software dello Strato Middleware
Type:	Technical document
Status:	Under development
Description:	This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signalling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.
Title:	Design architetturale dello strato Middleware
Type:	Technical document
Status:	Under development
Description:	This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signalling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.

Title: MASK - Middleware tra Applicativi Software e Kernel
Type: Software library
Status: Under development
Description: This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI), the Consorzio Interuniversitatio Nazionale per l'Informatica (CINI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI). which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. The object in question is a software layer used in the context of railway control and signalling systems. Its purpose is to allow a set of railway application logic to carry out their tasks without having direct dependencies on the operating system and hardware on their processing node. The software has been designed to be distributed on the various and different systems in the railway context.

Title: Design and Implementation of a Hardware/Software Redundancy Management System for Fail-Safe Control
Type: Journal article
Status: Still writing
Abstract: Physical redundancy is a common approach to improve the dependability of safety-critical systems, i.e. systems whose failure can cause serious damage to the economy, the environment and/or people. In some application domains it is possible to exploit the existence of a fail-safe state to reduce the implementation costs of a redundant system, using fault-detection and isolation techniques instead of fault-masking. In this paper is proposed the implementation of a software system for the management of physical redundancy on two-out-of-two architecture that facilitates the implementation of the application logic, making it unaware of the redundancy both in terms of synchronization and voting process leveraging Real-Time Operating System (RTOS) features, such as inter-process communication mechanisms. The proposed mechanisms have been implemented both on general-purpose operating system, consisting of a real-time patch of GNU/Linux, and on two RTOS for small processors and microcontrollers typically used in industry, demonstrating to be independent from the hardware architecture, from the particular RTOS and easily implementable w.r.t. the software development regulations for the industrial domain of reference.

Hardware security and trust

Title: Enforcing mutual authentication and confidentiality in Wireless Sensor Networks using Physically Unclonable Functions: a case study
Type: Master Thesis (as Co-rapporteur)
Status: Released

Title: Enforcing mutual authentication and confidentiality in Wireless Sensor Networks using Physically Unclonable Functions: a case study
Type: Journal article
Status: Still writing
Abstract: The technological progress we witnessed in recent years has led to a substantial reduction in hardware costs, which allows intelligent devices to be used for applications that were previously precluded. The monitoring of Power Delivery Networks (PDNs) is an example: the use of interconnected sensors makes it possible not only to detect faults, but also to adapt the network topology to isolate and compensate for them. In this paper we discuss how Fault-Detection, Isolation and Service Recovery (FDISR) for PDNs can be modeled according to the fog-computing paradigm, which distributes part of the intelligence and computation burden among edge nodes, while adopting cloud services only for heavy-weight computation. In particular, we consider an FDISR application on Medium-Voltage PDNs (MV-PDNs), which feed industrial users that, in cases of interrupted power supply, can suffer considerable damages. A Wireless Sensor Network (WSN) whose nodes make use of the Long Range (LoRa) technology to communicate with each other is considered, combining the cost-effectiveness and ease of installation of WSN with long-range coverage and reliability. Security concerns and the attack model of such application are discussed, then the use of a communication protocol based on the Physically Unclonable Functions (PUFs) mechanism is proposed to achieve both mutual authentication and confidentiality. Finally, an implementation of the proposal is presented and evaluated w.r.t. security concerns and communication overhead..