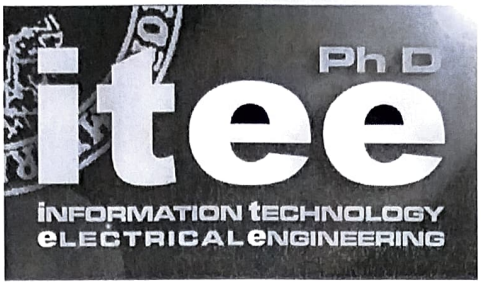



**PhD in Information Technology and Electrical Engineering**

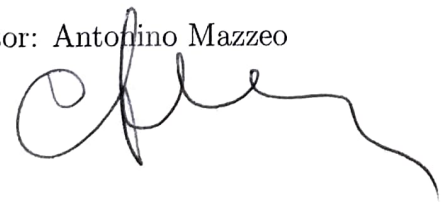
**Università degli Studi di Napoli Federico II**

PhD Student: Salvatore Barone

XXIX Cycle

**Training and Research Activities Report – First Year**

Tutor: Antonino Mazzeo



UNIVERSITÀ DEGLI STUDI DI NAPOLI
FEDERICO II

# 1 Study and Training activities

This section lists all the courses and seminars I have attended during the last year. The list does not follow a chronological order.

## Courses

| | |
|---|---|
| **Title:** | Intelligenza Artificiale |
| **Date:** | 11/2018 - 12/2019 |
| **Lecturer(s):** | Flora Amato |
| **Credits Earned:** | 6 |

| | |
|---|---|
| **Title:** | Advanced techniques for software robustness and security testing |
| **Date:** | 16/01/2019, 30/01/2019, 13/02/2019, 20/02/2019, 07/03/2019, 19/03/2019, 02/04/2019 |
| **Lecturer(s):** | Roberto Natella |
| **Credits Earned:** | 3 |

| | |
|---|---|
| **Title:** | Green Economy and Management in Engineering Projects |
| **Date:** | 8-12/07/2019 |
| **Lecturer(s):** | G.Zollo, C.Piccolo, G.Ferruzzi, P. De Falco, G.M. Mauro, P. Rippa |
| **Credits Earned:** | 3 |

## Seminars

| | |
|---|---|
| **Title:** | How to publish a scientific paper |
| **Date:** | 26/11/2019 |
| **Lecturer(s):** | Aliaksandr Birukou, Elisa Magistrelli |
| **Credits Earned:** | 0.4 |

| | |
|---|---|
| **Title:** | Bitcoin e blockchain oltre l'hype |
| **Date:** | 18/01/2019 |
| **Lecturer(s):** | G.Sabbatini, L. Giustozzi, M.Monaco, F.Balsamo |
| **Credits Earned:** | 0,6 |

| | |
|---|---|
| **Title:** | Matlab and Embedded Systems |
| **Date:** | 28/03/2019 |
| **Lecturer(s):** | Stefano Marrone |
| **Credits Earned:** | 0,4 |

### Extended courses

| | |
|---|---|
| **Title:** | Cambridge English Level 2 Advanced Certificate |
| **Date:** | 01/2019 - 06/2019 |
| **Reference Number:** | 196IT5885004 |

# 2 Research activities

Currently, my research activity focuses on three main themes: the design and development of safety-critical applications in the railway domain, approximate computing for software applications and for hardware circuits, hardware-security and trust. In the following, they will be discussed in detail.

**The railway domain** With regard to applications in the railway sector, I initially continued my thesis work, studying an innovative architecture for redundant safety-critical systems in the railway sector, as part of a joint project involving DIETI and RFI - Gruppo delle ferrovie dello Stato S.p.a.. This research activity is still ongoing, but it has produced several intermediate products, such as the reliability assessment for some hardware peripherals, a document specifying the software requirements, a document on architectural design and a working prototype of the system. To this activity, the design and implementation of a software library for the Automatic Train Operator was added. This activity is also still in progress, but a document specifying the requirements, the source code of the software, has been produced. The latter has also been tested on the target architecture. Moreover, one thesis work has been completed and two more are in progress on this activity.

**Approximate Computing** Approximate Computing is a new design paradigm that has been introduced to achieve better computational or energy performances by relaxing functional specifications of a system. It exploits the existing gap between the accuracy level provided by computer systems and the one really needed by applications, or the end-users, with the latter being lower than the former. This means that a large variety of applications could potentially benefit from it. Leveraging the full potential of Approximate Computing requires addressing several issues and challenges: there is no generic methodology, no generic approach and none of the techniques proposed in the scientific literature have general applicability. My research activity focuses on the definition of a general methodology and the development of an automatic and generic tool that can help designers in assessing the trade-off between error and performance gain.

**Hardware security and trust** The subject is vast and it would not be enough to have a book to talk about it. My research activity concerns mutual authentication protocols implemented using Physical Unclonable Functions (PUFs). In particular, the implementation of a protocol to allow sensor nodes of a wireless sensors network to authenticate themselves while communicating.

# 3 Products

In this section are listed all the works I have written - or am still writing - during the last year. The list is organized by research topic and does not follow a chronological order.

## The railway domain

| | |
|---|---|
| **Title:** | Libreria Interfacce I/O ATO - Definizione dell'architettura |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use. |

| | |
|---|---|
| **Title:** | Interazione e comunicazione tra task applicativi in ambiente Safety Critical |
| **Type:** | Master Thesis (as Co-rapporteur) |
| **Status:** | Released |
| **Description:** | |

| | |
|---|---|
| **Title:** | SCSC - Sistema Controllo e Smistamento delle Comunicazioni |
| **Type:** | Software library |
| **Status:** | Released, a new version is under development |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use. |

| | |
|---|---|
| **Title:** | Manuale d'uso e istallazione della libreria SCSC |
| **Type:** | User Manual |
| **Status:** | Released, a new version is under development |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build a prototype for a Unmanned Railway Vehicle (URV) for the monitoring and maintenance of the high-speed railway line. In particular, the research activity refers to the design and development of a prototype for a software library that abstracts all the communication mechanisms that the railway logic can use. |

| | |
|---|---|
| **Title:** | Gigabit Ethernet Controller su dispositivi della famiglia Xilinx Zynq-7000 e Ultrascale+ |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. |

| | |
|---|---|
| **Title:** | Implementazione della Comunicazione con Protocollo Serial Peripheral Interface su Dispositivi della Famiglia Xilinx Zynq-7000 |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. |

| | |
|---|---|
| **Title:** | UART Controller su dispositivi della famiglia Xilinx Zynq-7000 e Ultrascale+ |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. |

| | |
|---|---|
| **Title:** | Specifica dei Requisiti Software dello Strato Middleware |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. |

| | |
|---|---|
| **Title:** | Design architetturale dello strato Middleware |
| **Type:** | Technical document |
| **Status:** | Released |
| **Description:** | This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology. |

**Title:** MASK - Middleware tra Applicativi Software e Kernel
**Type:** Software library
**Status:** Under development
**Description:** This work is part of a joint project between the Dipartimento di Ingegneria Elettrica e delle Tecnologie dell'Informazione (DIETI) and the Rete Ferroviaria Italiana - Gruppo delle Ferrovie dello Stato S.p.a (RFI) which aims to design and build an ERTMS/ETCS propotype system on hybrid ARM/FPGA technology.

## Approximate computing

**Title:** Approximate Computing by Mutation: a General Approach
**Type:** Journal article
**Publisher:** IEEE Transaction on Computers
**Status:** Under Review
**Abstract:** Traditional computing system design paradigm is no more adequate to guarantee significant performance enhancement against affordable effort, while computational resource demanding of modern applications is rising to unprecedented levels. Indeed, since current Integrated Circuit (IC) manufacturing technology is dramatically close to its physical limit, die-shrinking is going to be not a suitable solution. So far, Approximate Computing (AxC) has been introduced to achieve better computational performances by relaxing functional specifications of a system. The idea behind AxC is to trade quality output results off for execution time, energy consumption and, for IC, area reduction. In this paper, we propose a generic framework based on the concept "approximate by mutation", implemented in the IDEA tool-suite, that makes use of genetic searching algorithm to detect best approximate variants of a given C/C++ implemented algorithm. In order to prove the effectiveness of the proposed approach, we give a detailed walk-through for implementing an efficient hardware accelerator for approximate Discrete Cosine Transform (DCT). Experimental results over different hardware configurations show a reduction of required area of about 15% and a reduction in power consumption of about 60% on two different technology targets, namely Field Programmable Gate Array (FPGA) and Application Specific Integrated Circuit (ASIC)

| | |
|---|---|
| **Title:** | Advancing Synthesis of Decision Tree Based Multiple Classifier Systems: an Approximate Computing Case Study |
| **Type:** | Journal article |
| **Status:** | Still writing |
| **Abstract:** | So far, multiple classifier systems have been increasingly designed to take advantage of hardware features, such as high parallelism and computational power. Indeed, compared to software implementations, hardware accelerators guarantee higher throughput and lower latency. Although the combination of multiple classifiers leads to high classification accuracy, the required area overhead makes the design of a hardware accelerator unfeasible, hindering the adoption of commercial configurable devices. For this reason, in this paper, we exploit Approximate Computing design paradigm to trade hardware area overhead off for classification accuracy. In particular, employing bit-width reduction technique, we explore approximate decision tree variants by means of multiple objective optimization problem, demonstrating a significant performance improvement targeting a Xilinx Zynq 7020 field programmable gate array device. |
| **Title:** | Design space exploration tools for Approximate Computing |
| **Type:** | Book chapter |
| **Publisher:** | Springer |
| **Status:** | Still writing |
| **Description:** | This work collects the state of the art regarding approximate computing techniques and automatic tools for the design and evaluation of software applications and hardware circuits. The scientific literature on the subject is carefully summarized, in order to provide the reader with a broad and detailed knowledge of the subject. The chapter includes a detailed description of the IDEA tool-suite and its operation, including an example of use. In addition, there are several ideas for the future of research in this area. |

| | |
|---|---|
| **Title:** | Reconfigurable hardware designs: analysis and implementation of approximate JPEG compression variants |
| **Type:** | Master Thesis (as Co-rapporteur) |
| **Status:** | Completed |
| **Abstract:** | One of the most promising fields of application for Approximate Computing (AxC) is image processing, because of the high redundancy commonly present in the images and of the action of median filter performed by the human eye. For this field, the JPEG is one of the most frequently used lossy methods. It is based upon the Discrete Cosine Transform (DCT) algorithm as a basic processing step, to convert images into the frequency domain. Many different fast algorithms for DCT computation have been proposed for image applications, although they still use floating-point arithmetic for result computations. In this manuscript, in order to simulate the effect of AxC techniques over several DCT algorithms, a software model has been devised. This model is suitable for the generation of a hardware design, therefore, the subsequent hardware project can be reconfigurable in terms of the inner composition of the arithmetic units. By the usage of automatic tools based upon Genetic Algorithm, all the variants given by the parametrization of the reconfigurable variables have been explored, in order to find out a set of dominant hardware configurations. These configurations have been deployed on two different technologies, the first one is the FPGA, the second one is the ASIC; subsequently, a series of reports has been summarized, to be able to trace the area requirements and an energetic profile of each hardware component. |

| | |
|---|---|
| **Title:** | FPGA Synthesis of Approximate Logic Circuits for Embedded Applications |
| **Type:** | Master Thesis (as Co-rapporteur) |
| **Status:** | Still writing |
| **Description:** | This thesis aims to develop a general methodology for the automatic generation of approximate variants for non-arithmetic logic circuits, represented in low-level formats/languages, and the definition of appropriate metrics for the evaluation of the introduced degree of approximation and the obtained performance gains. |

## Hardware security and trust

| | |
|---|---|
| **Title:** | Efficient reed-muller implementation for fuzzy extractor schemes |
| **Type:** | Conference paper |
| **Publisher:** | Proceedings - 2019 14th IEEE International Conference on Design and Technology of Integrated Systems In Nanoscale Era, DTIS 2019 (2019) |
| **Status:** | Published |
| **Abstract:** | Nowadays, physical tampering and counterfeiting of electronic devices are still an important security problem and have a great impact on large-scale and distributed applications, such as Internet-of-Things. Physical Unclonable Functions (PUFs) have the potential to be a fundamental means to guarantee intrinsic hardware security, since they promise immunity against most of known attack models. However, inner nature of PUF circuits hinders a wider adoption since responses turn out to be noisy and not stable during time. To overcome this issue, most of PUF implementations require a fuzzy extraction scheme, able to recover responses stability by exploiting error correction codes (ECCs). In this paper, we propose a Reed-Muller (RM) ECC design, meant to be embedded into a fuzzy extractor, that can be efficiently configured in terms of area/delay constraints in order to get reliable responses from PUFs. We provide implementation details and experimental evidences of area/delay efficiency through syntheses on medium-range FPGA device. |

# 4 Conferences and Seminars

| Date | Place | Title |
|---|---|---|
| 15-18/04/2019 | Mykonos, Greece | 14th IEEE International Conference on Design and Technology of Integrated Systems In Nanoscale Era, DTIS 2019 |
| 30/09/2019 - 01/10/2019 | Naples, Italy | The Italian Workshop on Embedded Systems, IWES 2019 |

# 5 Activity abroad

| Date | Place | Subject |
|---|---|---|
| 18-20/12/2018 | Firenze, Polo Ferroviario dell'Osmannoro | On-board subsystem for ERTMS/ETCS |
| 14-16/01/2019 | Firenze, Polo Ferroviario dell'Osmannoro | On-board subsystem for ERTMS/ETCS |
| 25-26/02/2019 | Pisa - Istituto di Tecnologie della Comunicazione dell'Informazione e della Percezione | Real-time Operating Systems |
| 27/02/2019 | Firenze - Polo Ferroviario dell'Osmannoro | The Automatic Train Operator and the SCSC software library |
| 15-17/09/2019 | Firenze - Polo Ferroviario dell'Osmannoro | The Automatic Train Operator and upgrades for the SCSC software library |