PhD in Information Technology and Electrical Engineering

Università degli Studi di Napoli Federico II

PhD Student: Vida Abdolzadeh

XXXII Cycle

Training and Research Activities Report – First Year

Tutor: Nicola Petra

1. Information

I graduated in Computer Engineering; currently, I am attending the first year of PhD in Information Technology and Electrical Engineering - ITEE XXXII Cycle at the University of Naples Federico II, under the supervision of Prof. Nicola Petra. I was winner scholarship for international student .

2. Study and Training activities

In this first year I followed courses to improve knowledge in system on chip and digital electronics devices (through PhD Schools), courses to improve research skills (through ad hoc modules of ITEE PhD), course to improve English language and to broaden my knowledge in topic near digital electronics (through M. S. courses and Occasionally provided courses of ITEE PhD).
To be more specific:

a. Courses
   - (3 CFU) Satellite Remote Sensing: open challenges and opportunities – Prof. Giuseppe Ruello – 23-31/10/2017
   - (9 CFU) System on Chip – Prof. Nicola Petra – 08/01/2018
   - (9 CFU) Power devices and circuits– Prof. Ettore Napoli – 05/12/2017

b. Seminars
   - (1 CFU) Optimal control of networks: energy scaling and open challenges –Prof. Francesco Sorrentino –20/12/2017
   - (1 CFU) Optimal Content Distribution and Multi-Resource Allocation in Software Defined Virtual CDNs – Prof. A.M.Tulino and C.Sterle – 12/12/2017
   - (0.8 CFU) (Effective) Machine Learning in the Time of Big Data – Prof. Anna Corazza – Ing- Matteo Santoro – 28/11/17
   - (0.4 CFU) The estimation of the cost of software development projects – prof. Carlo Sansone – 5/5/2017
   - (0.4 CFU) Exploiting Speech Production Knowledge for Deep earning based Automatic Speech Recognition – prof. Francesco Cutugno – 9/5/2017
   - (0.4 CFU) Complex Dynamics in Memristor Networks: Flux-Charge Analysis Method and Bifurcations without Parameters – prof. Mario Di Bernardo - 15/5/2017

	Credits year 1							
		1	2	3	4	5	6	
	Estimated	bimonth	bimonth	bimonth	bimonth	bimonth	bimonth	Summary
Modules	20	0	0	0	0	3	9	**12**
Seminars	5	0	1.2	0	0	0.8	2	**4**
Research	35	10	8.8	10	8	6.2	1	**44**
	60	10	10	10	8	10	12	**60**

3. Research activity

My research activity is actually focused on Neural network. Neural network are widely used today for image and speech recognition. Speech recognition is used to allow the interaction between human and electronics devices using the voice. This feature is becoming widely used and required. The implementation of a neural network relies on the use of powerful high-end elaboration systems. The usual solution requires the use of several servers running the neural network software, and the interaction between the user and the servers is achieved by means of an internet connection.

There are several applications that do not allow the use of high-end computers nor the use of an internet connection. For instance, using neural networks on a car is problematic because the connection to the internet cannot be guaranteed. Furthermore, the use of speech and image recognition in the domestic devices (smart television, smart refrigerator, etc.) cannot make use of an external network because of security reasons.

For these reasons there is a strong interest in the implementation of neural networks using low cost, mid power, electronic devices. The most promising technology to be used to that purpose are Systems on Chip, which are integrated circuits that provide, on the same chip, one or more processors and dedicated application specific circuitry. However, the modification to be applied to the neural network algorithms in order to make them implemented with a System on Chip is not trivial.

The purpose of my research activity is to investigate trade-offs and architectures that can be used for the implementation of neural network ready Systems on Chip.

From an algorithmic point of view, a neural network is obtained as the sequence of similar mathematical operations, called layers. The derivation of an efficient circuit for the implementation of the single layer is mandatory for the implementation of the whole network.

My activity for the next months is focused on the development of efficient circuits for the implementation of the so-called Long Short Term Memory layer, which is widely used in many speech recognition networks.